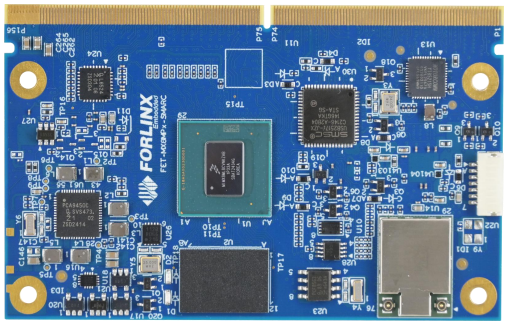
FET-MX8MPQ-SMARC SoM

It is developed and designed based on the NXP i.MX8M Plus processor, which focus on machine learning and vision, advanced multimedia, and industrial automation with high reliability. It aims to meet the requirements of applications such as smart cities, industrial IoT, intelligent healthcare, and intelligent transportation. It features a strong quad - core Arm Cortex - A53 processor (up to 1.6 GHz), an NPU (up to 2.3 TOPS), 1 x ISP and 2 x camera inputs for an efficient vision system. Multimedia includes H.265 video encoding/decoding, 3D/2D graphics acceleration and audio/voice functions. Real - time control via Cortex - M7, a CAN FD and dual Gigabit Ethernet control network with TSN. High - speed interfaces like 2 x USB 3.0, 1 x PCIe 3.0 and 1 x SDIO 3.0 serve 5G, HD video, dual - band WiFi and high - speed industrial Ethernet.



Product Features:

- Multi - core heterogeneity, 1.6GHz main frequency
- Dual Gigabit Ethernet, with 1 x supporting TSN
- Powerful multimedia functions supporting 3D/2D graphics acceleration
- Built - in NPU, 2.3TOPS AI computing
- Built - in ISP, dual camera inputs for advanced vision
- Various configurations, stable OS

4×A53+M7 Architecture	1.6 GHz Main Frequency	2.3TOPS NPU
CAN-FD 2	TSN Ethernet	-40℃~+85℃ Temperature Range

SoM Basic Parameters:

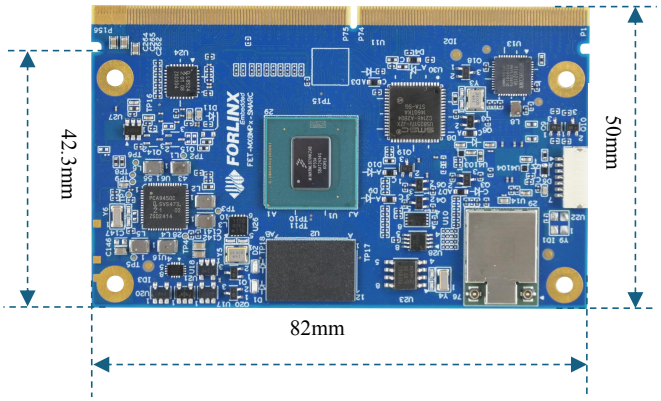
Processor	**NXP i.MX8MPQ** **CPU:** 4×Cortex-A53@1.6GHz+Cortex-M7@800MHz **GPU:** Supports 3D and 2D GPU, OpenGL ES 1.1, 2.0, 3.0, OpenCL 1.2, Vulkan **NPU:** 2.3TOPS **VPU:** **Hardware Decoding:** HEVC/H.265, VP9, VP8, AVC/H.264:up to 1080p@60fps **Hardware Encoding:** H.265/HEVC, H.264/AVC:up to 1080p@60fps
RAM	2/4 GB LPDDR4
ROM	16/32 GB eMMC
Working Voltage	5V
Operating Temperature	-40℃~+85℃
Interface	SMARC2.1 （314pin, Body Height-7.8mm, Stack Height-5mm）

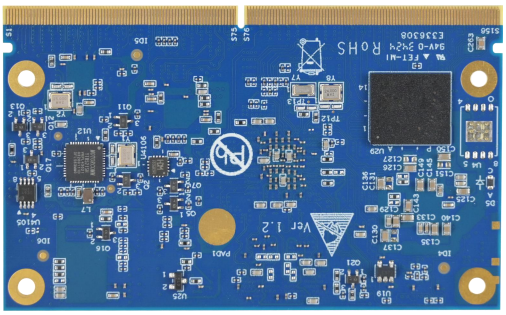
SoM Function Parameters:

Function	Quantity	Parameter
USB 3.0	2	2 x USB 3.0/2.0 controllers with integrated PHY.
USB 2.0	5	Supports Highspeed (HS), Full-speed (FS), and Low-speed (LS)
MIPI CSI	2	2 x 4-lane MIPI camera serial interfaces up to 1.5 Gbps.
MIPI DSI	1	1 x 4-lane MIPI display serial interface up to 1.5 Gbps operation 1080 p60 • WUXGA (1920x1200) at 60 Hz 1920x1440 at 60 Hz UWHD (2560x1080) at 60 Hz WQHD (2560x1440) by reduced blanking mode （Simplified Cloaking Mode）
LVDS	2	Supports resolutions up to 1920x1080p60
HDMI	1	Supports resolutions up to 4kp30
Ethernet	2	EMAC supports 10/100/1000 Mbps data transfer rates, with 1 x supporting TSN.
PCIe	1	Supports PCI Express Gen 3
CAN-FD	2	CAN FD controller, compatible with CAN 2.0B and ISO 11898-1.
SDIO	1	Supports SDIO 3.0
IIS	2	SAI supporting full-duplex, frame-synchronized serial interfaces including I2S, AC97, tdM and codec/DSP.
SPI	2	Max data rate up to 52 Mbit/s; configurable master/slave modes.
IIC	5	Max data rate up to 320 kbps.
UART	4	Baud rate up to 4Mbps.
PWM	3	Features a 16-bit counter.
GPIO	>14	
WiFi & BT	1	Supports Wi-Fi 5 MIMO and Bluetooth 5.3, directly connected to the processor via SDIO 3.0 and UART interfaces.
JTAG	1	Complies with IEEE 1149.1 testability (JTAG) standard.

Note: The parameters in the table are hardware design or theoretical CPU values.

Appearance and Dimensions:





Note: Dimensions marked with * have a tolerance of ±0.2 mm.

Software Support:

OS	**Linux 6.1.36+Qt6.5.0**
Flashing Method	**USB OTG**

Peripheral Support List:

Linux 6.1.36 Driver Support List	**Interface**	**Function**	**Plan**
	SIDO	WiFi	On-board AW-CM276NF
	UART	Bluetooth Module	
	IIS	Audio	NAU8822
	IIC	RTC chip	PCF8563
	MIPI-DSI	7" Capacitive Touch Screen	FIT-LCD7.0_MIPI V2.1
	IIC	Touch ft5306	
	LVDS	10.1" Capacitive Touch Screen	FIT_LVDS_10.1_C
	IIC	Touch gt928	
	USB	4G Module (M.2 package)	EM05-CE (China), EM05-G (Global)
	USB	5G Module (M.2 package)	RM500U-CN (China), RM520N-GL (Global)
	USB	USB camera	Logitech C270
	PCIe	PCIe NIC	INTEL E1000
	MIPI-CSI	MIPI camera	OV5645
	MIPI-CSI	MIPI camera	daA3840-30mc

Product Material List:

Linux6.1.36 Material List	User's Manual, Compilation Guide, Linux Kernel Source Code, File System, Factory Image, SD card flashing tool, USB OTG flashing tool, Qt test example source code, application notes.*
Hardware Materials List	Hardware Manual, Carrier Board Schematics Source File (AD format), Carrier Board PCB Source File (AD format), Chip Data Manual, SoM & Carrier Board 2D CAD Drawing, Pin Function Multiplexing Table, Design Guide*

Note: Comprehensive materials will be provided after release.

Order Model List:

Specification Model	**SoM**	**CPU Clock**	**RAM**	**ROM**	**Operating Temperature**	**Supply**
FET-MX8MPQ-SMARC+162GSE16GIxx:xx	4×A53	1.6 GHz	2GB	16GB	-40℃~+85℃	SOP
FET-MX8MPQ-SMARC+164GSE32GIxx:xx	4×A53	1.6 GHz	4GB	32GB	-40℃~+85℃	SOP

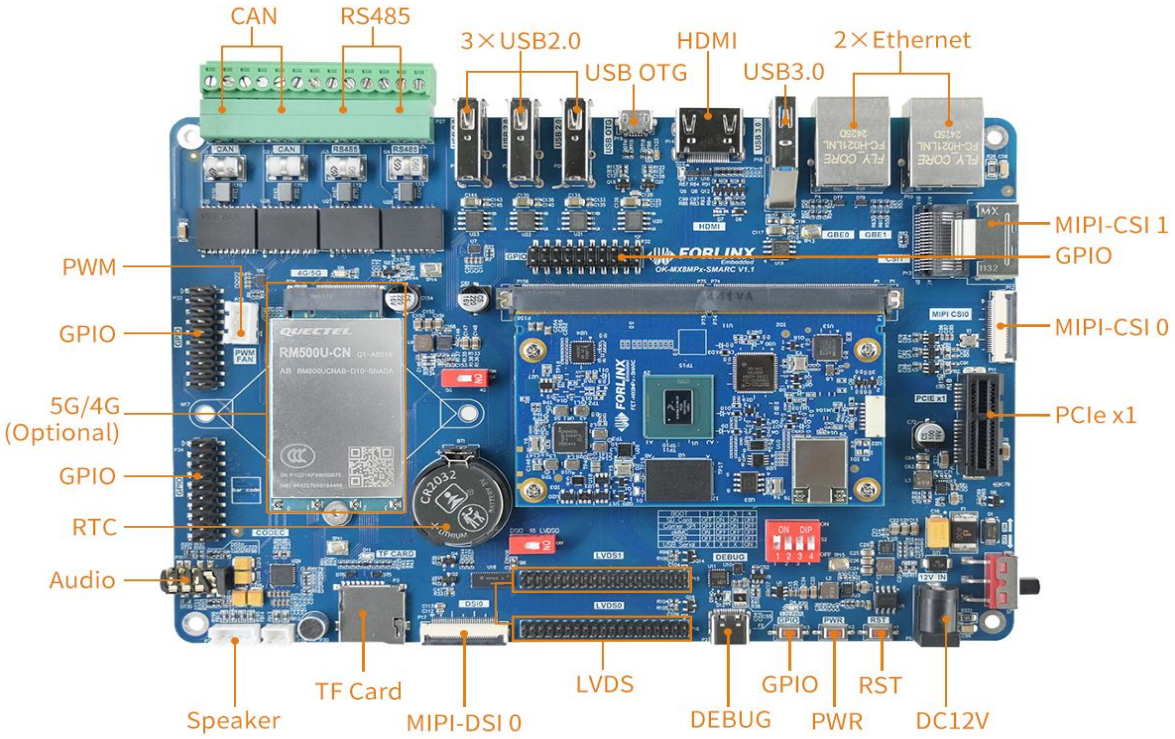
SoM Naming Rule:

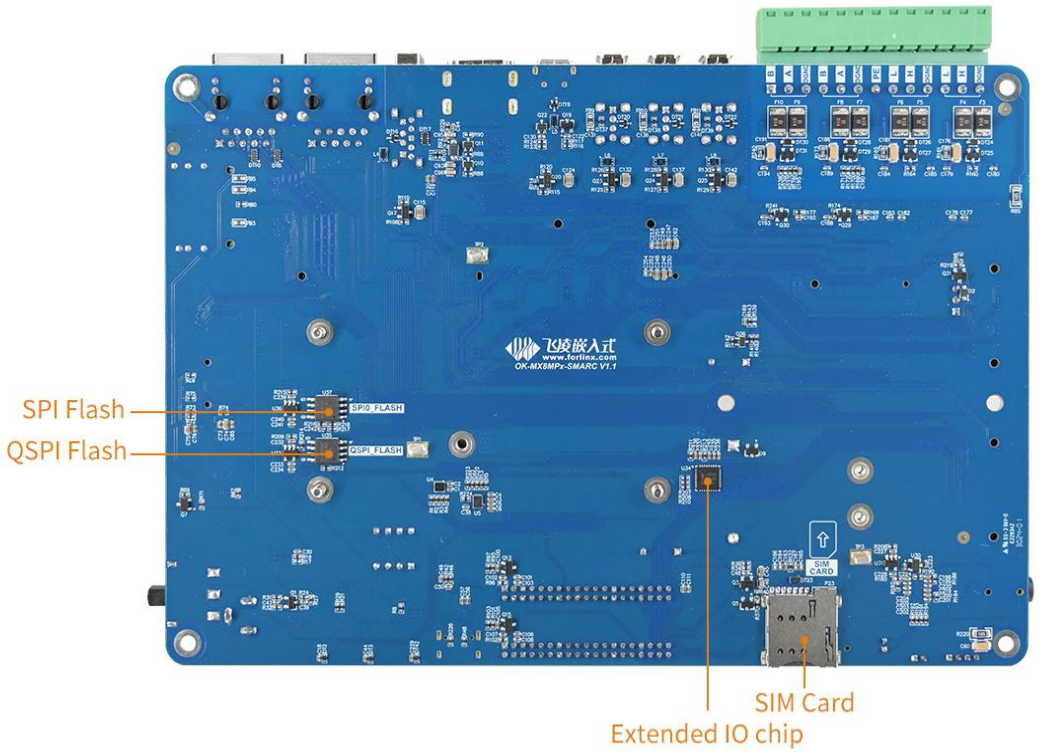
A	-	B	-	C	+	D	E	F	G	H	I	J	:	K	L

This table describes the terminology used for SoM numbering to identify the features of the SoM (such as CPU, frequency, temperature grade, version, etc.).

Field	Field Description	Value	Description
A	Product Line Identification	FET	Folinx Embedded SoM
-	Segment Identification	-	
B	CPU	MX8MPQ	i.MX8MPQ
-	Segment Identification	-	
C	Connection	SMARC	SMARC 2.1
+	Segment Identification	+	This identifier is followed by the configuration parameter.
D	CPU clock	16	1.6 GHz
E	RAM Capacity	2G	2GB
	(Unit: Byte)	4G	4GB
F	Single ROM Type	SE	eMMC
	Multiple ROM Type	OE	Nor Flash + eMMC
G	Single ROM Capacity	16G	16GB
	(Unit: Byte)	32G	32GB
H	Operating Temperature	I	-40℃ to +85°C Industrial Grade
I	Configuration No.	A~Z	If D-H field values are identical across products, they are treated the same and sorted by release time in ascending order.
J	PCB Version	10	V1.0
		11	V1.1
		xx	Vx.x
:KL	Manufacturer's Internal Logo	:xx	It is manufacturer's internal logo without influence on use.

Development Board





Function Parameters

Function	Quantity	Parameter
USB 3.0	1	USB Type A connector: Serves only as HOST. Load switch with over - voltage and over - current protection.
USB 2.0	3	USB Type A connector: Serves only as HOST. Load switch with over - voltage and over - current protection.
USB 2.0 OTG	1	USB Type C connector: Function switchable between HOST and SLAVE via DIP switch. Load switch with over - voltage and over - current protection. Available for USB programming.
MIPI CSI	2	CSI1: Supports daA3840 - 30mc camera module (resolution: 3840X2160). CSI0: Dual data channels, led out via 26Pin FPC socket. Supports OV5645 module.
MIPI DSI	1	Per SMARC protocol, function switchable between DSI0 and LVDS0 via Switch chip. 4 - lane MIPI DSI led out via FPC socket. Compatible with 7 - inch Forlinx MIPI screen (1024×600@30fps).
LVDS	2	Per SMARC protocol, function switchable between DSI0 and LVDS0 via Switch chip. It supports 2 sets of 4 - lane LVDS 1080P displays with LVDS0/DSI0 sharing data channels, and is compatible with Forlinx's 10.1 - inch LVDS screen.
HDMI	1	Supports HDMI 2.0a with a display resolution up to 3840 x 2160@30fps.
Ethernet	2	Supports 10/100/1000Mbps self-adaption, led out via RJ45 interface, with 1 x supporting TSN; The development board uses a standard PCIE x1 card interface, supporting PCI Express Gen3.
TF Card	1	Dev board supports 1 x SDIO for UHS - I TF cards, up to 104MB/s.
4G/5G	1	Dev board has M.2 B-KEY slot for 4G/5G selection. Default 4G: Quectel EM05, 5G: Quectel RM500. Insert SIM into onboard MicroSIM slot.
IIS	2	Dev board uses one IIS set to connect CODEC chip for Audio functions; Another IIS set is available on pin headers for expansion.
Audio	1	Default on-board NAU88C22YG chip, IIS interface; Supports headphone output and MIC input, integrated in a 3.5mm headphone interface; Supports 2 x 1W 8Ω speaker output via XH2.54 white terminal.
CAN-FD	2	Industrial isolated CAN - FD chip. Processor supports CAN - FD up to 8Mbps; Complies with CAN protocol version 2.0B specification; led out via DG128 green terminal;
QSPI	1	Dev board features 2 pcs 16MB FLASH chips, 1 using QSPI for communication.
SPI	1	Dev board features 2 pcs 16MB FLASH chips, 1 using SPI for communication, configurable for SPI boot.
RTC	1	The development board is equipped with a CR2032 coin cell battery to supply RTC power for the SoM. After the development board is powered off, the coin cell battery can be used to record time.
IIC	4	It is used to mount devices such as audio, cameras, and touchscreens on the development board.
Debug UART	2	2 x are converted into 1 x USB port for device debugging. The development board uses UART1 and UART2 for debugging.
RS485	2	The development board uses UART0 and UART3 for RS485 functionality. Industrial - grade isolated RS485 chip with a maximum speed of 4Mbps, and led out through DG128 green terminals.
PWM	5	Used to adjust the backlight brightness of the display screen and LED breathing lights;
GPIO	\	Multiple GPIO pins on the pin headers, including special - function pins specified by the SMARC protocol.

Note: The parameters in the table are hardware design or theoretical CPU values;