User's Manual

SoM FETMX8MPQ-C/ SBC OKMX8MPQ-C

ARM Cortex-A53+ Cortex-M7

Embedded Development Platform

Hardware Manual

Rev. 2.0

Forlinx Embedded Technology Co. Ltd. www.forlix.net

Attentions

MUST READ BEFORE WORKING WITH OKMX8MM-C

Product Operation Environment:

- Hot-plug of CPU module and peripheral modules is strictly prohibited.
- Please follow all the warnings and instructions marked on the product.
- Please keep the product dry. Once splashed or immersed by any liquid, cut off the power and dry it out immediately.
- Please store and operate the product in ventilating conditions to avoid damages brought by over high temperature.
- Please do not use or store the product in dusty or untidy conditions.
- Please do not use or store the product in alternate cold and hot conditions to avoid condensing which will damage components.
- Please do not treat the product rudely. Any falling-off, knocking and violate shaking may cause destruction to circuit and components.
- Please do not clean the product with organic solvents or corrodible liquids.
- Please do not dismantle or repair the product by yourself. Contact us when the product malfunctions.
- Please do not modify the product by yourself or use fittings unauthorized by us. Otherwise, the damage caused by that will be on your part and not included in guarantee terms.

Any questions please feel free to contact Forlinx Technical Service Department..

Copyright Announcement

Updating Record

Date	Version			Updated
	Manual	SoM	Carrier board	
Oct., 2021	V2.0	V1.0	V2.0	Carrier board PCB version updated to V2.0 1. PHY chip changed from AR8031-AL18 to YT8521; 2. Power circuited controlled by MOS, added with RC to avoid previous power drops during powering, including VSYS_5V, LVDS and audio power circuit on carrier board.
Aug., 2021	V1.0	V1.0	V1.1	First edition

Technical Support and Customization

1. Technical Support Range

1.1 Forlinx product related hardware and software source consulting;
1.2 Problems related to our software and hardware manual;
1.3 After-sale technical support for ODM product;
1.4 Forlinx product related trouble shooting, failure diagnose and related maintenance

2. Range of Technical Discussion (non-compulsory)

2.1 Modification and comprehension of source code;
2.2 How to implant OS;
2.3 Software and hardware problems occured in self-modifying and programming
Note: the above three points are out of Forlinx technical service range, but Forlinx will try best but can not promise to help users to solve the problems.

3. Accesses to Technical Support

3.1 If you are able to understand Chinese, you can try to all the technical persons directly, the tel. number (non-instant messenger) is 0086-312-3119192
3.2 Any Forlinx product related questions or help if you need, you can send email to corresponding sales engineer whom you keep in touch with, the sales engineer will help you to follow up your issue and get back to you soonest;
3.3 If you are not able to call the technical person and don't whom you should send email to, then you can send email to our public email address sales@forlinx.com or support@forlinx.com

4. Access to Materials

Forlinx product related technical files will be uploaded to dropbox, once users buy product from Forlinx, the sales engineer will provide users related product technical source download link;

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Chapter 1 Overview of NXP i.MX8MP SoC

The i.MX 8M Plus family is a set of NXP products focused on machine learning applications, combining state-of-art multimedia features with high-performance processing optimized for low-power consumption. The i.MX 8M Plus Applications Processor relies on a powerful fully coherent core complex based on a quad Cortex-A53 cluster, a Cortex-M7 coprocessor, audio digital signal processor, machine learning and graphics accelerators.

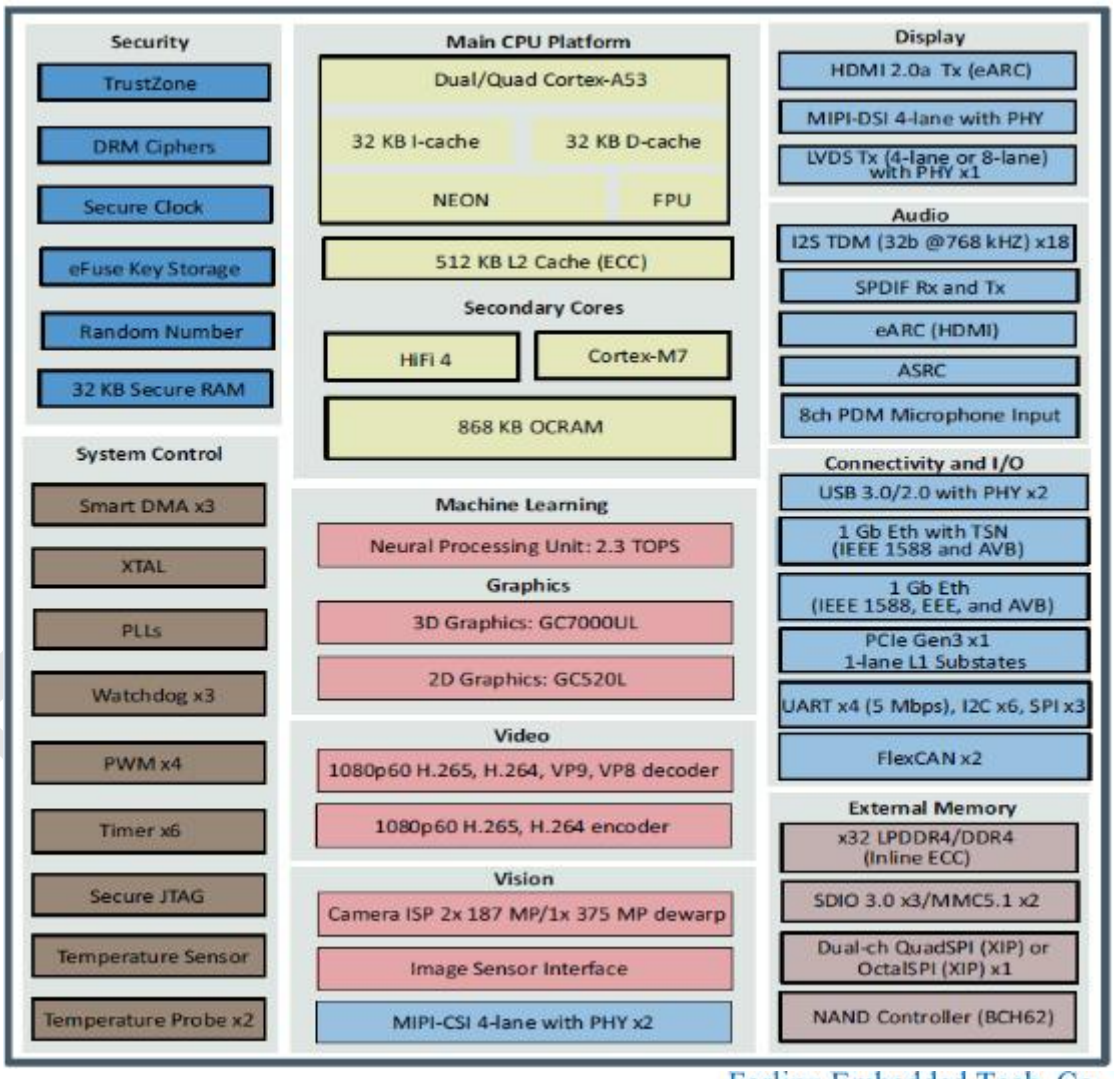
The i.MX 8M Plus provides additional computing resources and peripherals:

- Advanced security modules for secure boot, cipher acceleration and DRM support
- A wide range of audio interfaces
- Large set of peripherals that are commonly used in consumer/industrial markets including USB , PCIe, Ethernet, and CAN

Target Applications

The i.MX 8M Plus Media Applications Processor targets applications on:

• Smart Homes, Buildings and Cities
• Machine Learning and Industrial Automation
• Consumer and Pro Audio/Voice Systems



Forlinx FETMX8MPX-C SoM can support below CPU models, the standard one we use is MIMX8ML8CVNKZAB

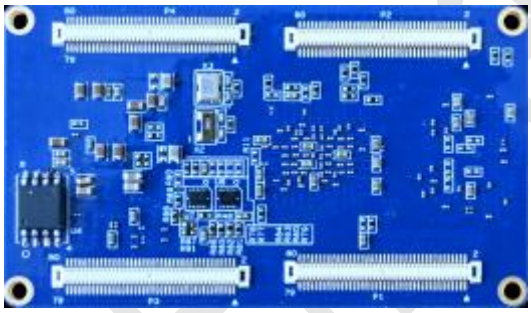
Part number	Device description	Part difference description	A53 Core number	A53 speed	Temp width
MIMX8ML8CVNKZAB	i.MX 8M PlusQuad	NPU, ISP, VPU,HiFi 4, CAN-FD	4	1.6 GHz	Industrial
MIMX8ML6CVNKZAB	i.MX 8M PlusQuad	ISP, VPU,CAN-FD	4	1.6 GHz	Industrial
MIMX8ML4CVNKZAB	i.MX 8M Plus QuadLite	CAN-FD	4	1.6 GHz	Industrial
MIMX8ML3CVNKZAB	i.MX 8M PlusDual	NPU, ISP, VPU,HiFi 4, CAN-FD	2	1.6 GHz	Industrial
MIMX8ML8DVNLZAB	i.MX 8M PlusQuad	NPU, ISP, VPU,HiFi 4, CAN	4	1.8 GHz	Consumer
MIMX8ML6DVNLZAB	i.MX 8M PlusQuad	ISP, VPU,CAN	4	1.8 GHz	Consumer
MIMX8ML4DVNLZAB	i.MX 8M PlusQuadLite	CAN	4	1.8 GHz	Consumer
MIMX8ML3DVNLZAB	i.MX 8M PlusDual	NPU, ISP, VPU,HiFi 4, CAN	2	1.8 GHz	Consumer

More details about the processor please refer to NXP website https://www.nxp.com.cn/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS

Chapter 2 Introduction of SoM FETMX8MPQ-C

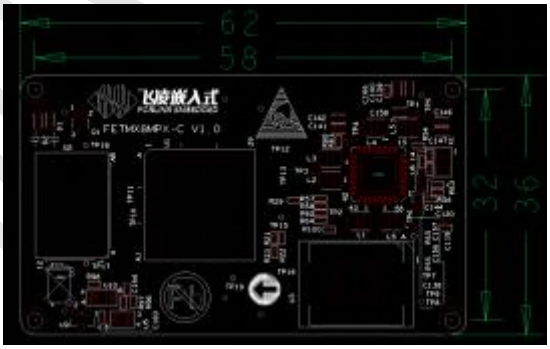
2.1 Exterior of SoM FETMX8MPQ-C

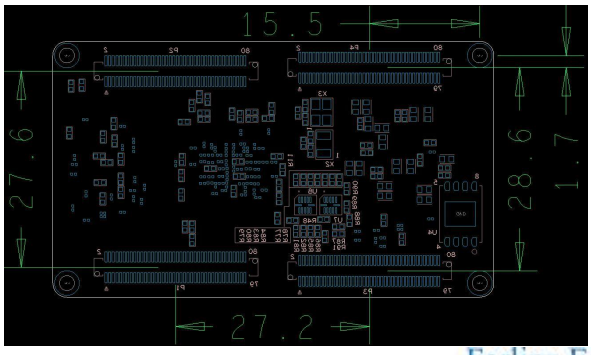
FETMX8MPQ-C



Note: FETMX8MPX-C is available for multiple processors, so it's printed as FETMX8MPX-C .

2.2 Dimension Drawing



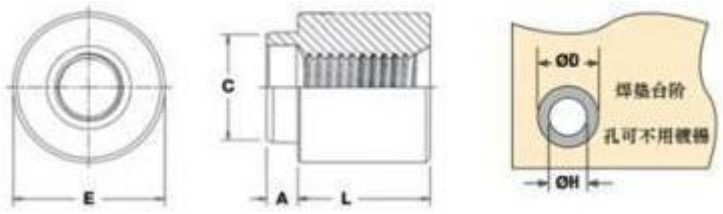


Dimensions: 36mm x 62mm, more details please fer to the DXF file.

PCB: ENIG, 8-layer, thickness: 1.6mm

Packing connector: four ultra thin 80-pin connectors with pitch of 0.5mm, SoM connector model AXK6F80337YG, carrier board connector AXK5F80537YG, the SoM is designed with four mounting holes with diameter of 2.2mm on the four corners.

Users can take Forlinx carrier board designing for reference, using M2, L=2mm mounting nuts as below



Thread size	Hole depth 0.1-0.08	Name	NO.	Length 'L'±0.1 Interval height code				Minimum thick	A maximum	C maximum	E ±0.1	Pore +0.08	Minimum Bonding pad
				1.8	2.5	3	5						
M2* 0.4	through-hole	smtsob	M2	2	3	4	6	1.53	1.53	3.6	5.56	3.73	6.2

2.3 SoM Parameters

2.3.1 Frequency

Item	Spec.				Note
	Minimum	Classic	Maximum	Unit	
Cortex-A53	--	--	1.6	GHz	Industrial grade
Cortex-M7	--	--	800	MHz	--

2.3.2 Power Supply

Item	Pin mark	Spec.				Note
		Minimum	Classic	Maximum	Unit	
Main power	VSYS_5V	4.5	5.0	5.5	V	--

2.3.3 Working Environment

Item		Spec.				Note
		Mini	Classic	Max	Unit	
Temp width	Working	-40	25	+85	℃	Industrial grade
	Storage	-40	25	+125	℃	
RH	Working	10	--	90	% RH	Non-condensing
	Storage	5	--	95	% RH	

2.3.4 SoM Interface Speed

Item	Spec.				Note
	Minimum	Classic	Maximum	Unit	
UART	—	115200	4M	bps	--
SPI	—	—	52	Mbps	
IIC	—	100	400	Kbps	--
CAN FD	—	—	8	Mbps	
SD/MMC/SDIO	—	—	800	Mbps	--
USB	—	--	5	Gbps	--
PCIe	—	—	8	Gbps	--

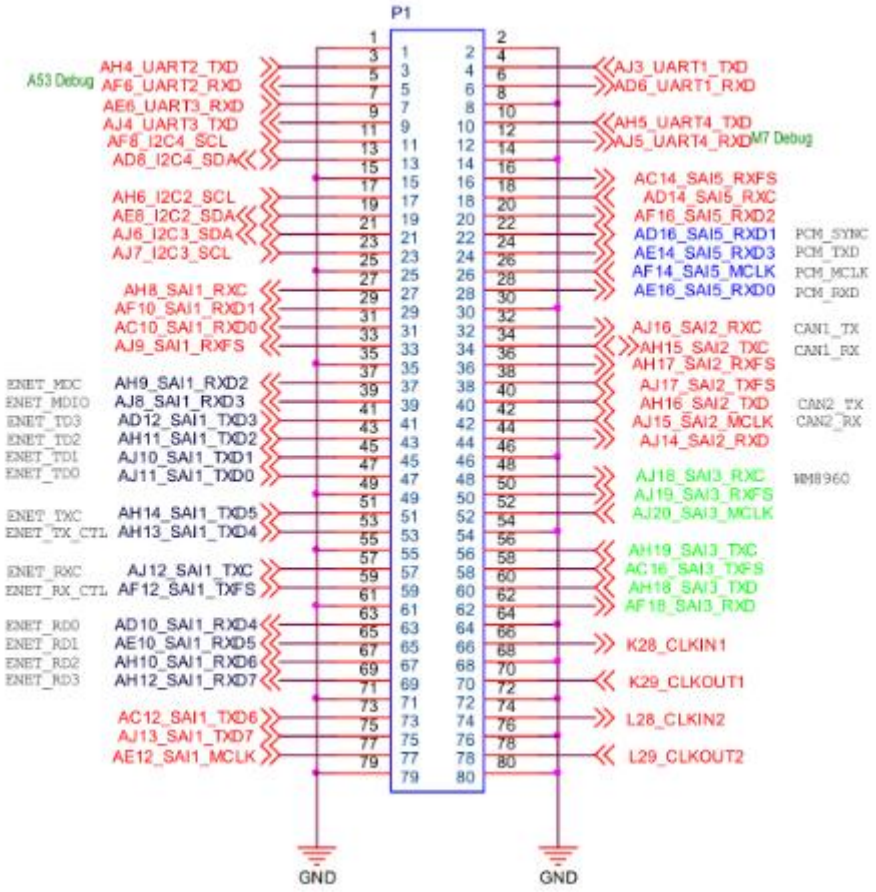
2.4 SoM Resource

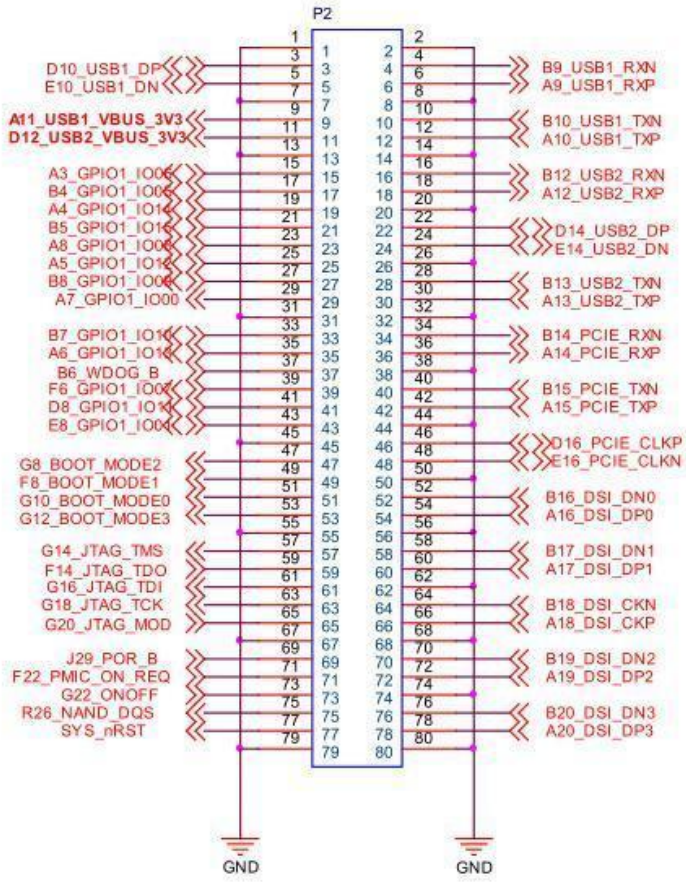
Peripheral	QTY	Spec.
USB	2	CPU integrated with 2 USB3.0/ 2.0 controllers both with PHY, can support Super-speed (5Gbit/s), high-speed(480Mbit/s), full-speed(12Mbit/s), low-speed(1.5Mbit/s) Device mode: SS/HS/FS
PCIe	1	PCI Express Gen3
MIPI_CSI	2	Two 4-lane MIPI CSI, up to 1.5Gbps
MIPI_DSI	1	One 4-lane MIPI DSI, up to 1.5Gbps • 1080 p60 • WUXGA (1920x1200) at 60 Hz • 1920x1440 at 60 Hz • UWHD (2560x1080) at 60 Hz • WQHD (2560x1440) by reduced blanking mode
HDMI	1	HDMI 2.0a, up to 4Kp30 HDMI2.1 eARC
LVDS	1	One 4-lane LVDS channel up to 7.0P60 Dual async channels(8 data, 2 clocks) 1920x 1200p60
Ethernet	≤2	2* RGMII, and one of them can support TSN
SD	≤2	SD2, 4-bit, 1.8/3.3V, SD1, 8-bit, 1.8V
UART	≤4	up to 4.0Mbps
SPI	≤3	up to 52Mbit/s, host and slave modes configurable

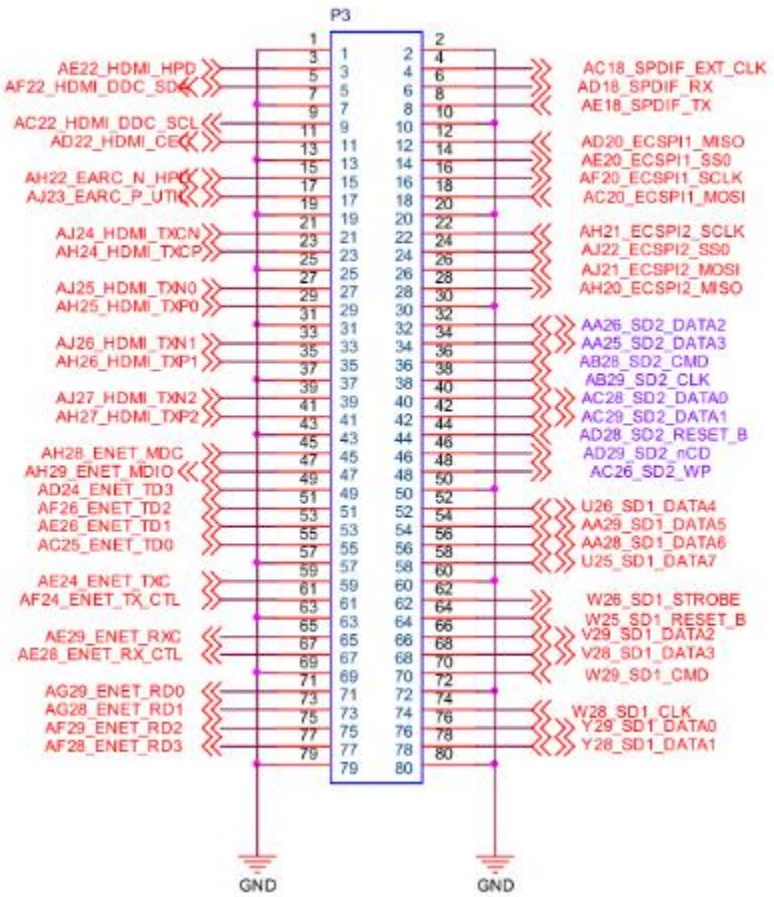
IIC	≤5	Standard mode up to 100Kbit/s; Fast mode up to 400Kbit/s
CAN	≤2	Comply with CAN FD protocol and also CAN2.0B.
SAI	≤6	Available for IIS, AC97, TDM and Codec/ DSP
SPDIF	≤1	S/ PDIF
PWM	≤4	16-bit upcounter;
JTAG	1	2x 5, pitch of 2.0mm headers
QSPI	≤1	Used by SoM, connected to 16MB Nor Flash

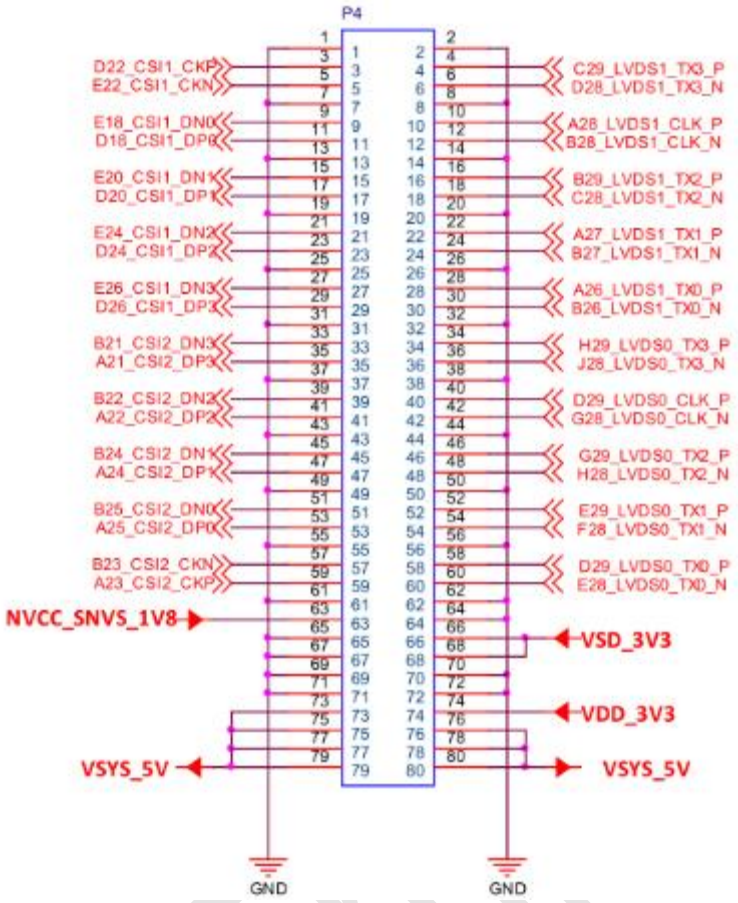
2.5 SoM FETMX8MPQ-C Pin Definition

2.5.1 SoM Connector Schematic




P2
D10_USB1_DP
E10_USB1_DN
A11_USB1_VBUS_3V3
D12_USB2_VBUS_3V3
A3_GPIO1_IO06
B4_GPIO1_IO05
A4_GPIO1_IO14
B5_GPIO1_IO15
A8_GPIO1_IO08
A5_GPIO1_IO13
B8_GPIO1_IO09
A7_GPIO1_IO00
B7_GPIO1_IO10
A6_GPIO1_IO11
B6_WDOG_B
F6_GPIO1_IO07
D8_GPIO1_IO12
E8_GPIO1_IO04
G8_BOOT_MODE2
F8_BOOT_MODE1
G10_BOOT_MODE0
G12_BOOT_MODE3
G14_JTAG_TMS
F14_JTAG_TDO
G16_JTAG_TDI
G18_JTAG_TCK
G20_JTAG_MOD
J29_POR_B
F22_PMIC_ON_REQ
G22_ONOFF
R26_NAND_DQS
SYS_nRST
B9_USB1_RXN
A9_USB1_RXP
B10_USB1_TXN
A10_USB1_TXP
B12_USB2_RXN
A12_USB2_RXP
D14_USB2_DP
E14_USB2_DN
B13_USB2_TXN
A13_USB2_TXP
B14_PCIE_RXN
A14_PCIE_RXP
B15_PCIE_TXN
A15_PCIE_TXP
D16_PCIE_CLKP
E16_PCIE_CLKN
B16_DSI_DN0
A16_DSI_DP0
B17_DSI_DN1
A17_DSI_DP1
B18_DSI_CKN
A18_DSI_CKP
B19_DSI_DN2
A19_DSI_DP2
B20_DSI_DN3
A20_DSI_DP3
GND
GND


P3
AE22_HDMI_HPD
AF22_HDMI_DDC_SDA
AC22_HDMI_DDC_SCL
AD22_HDMI_CEC
AH22_EARC_N_HPD
AJ23_EARC_P_UTIL
AJ24_HDMI_TXCN
AH24_HDMI_TXCP
AJ25_HDMI_TXN0
AH25_HDMI_TXP0
AJ26_HDMI_TXN1
AH26_HDMI_TXP1
AJ27_HDMI_TXN2
AH27_HDMI_TXP2
AH28_ENET_MDC
AH29_ENET_MDIO
AD24_ENET_TD3
AF26_ENET_TD2
AE26_ENET_TD1
AC25_ENET_TD0
AE24_ENET_TXC
AF24_ENET_TX_CTL
AE29_ENET_RXC
AE28_ENET_RX_CTL
AG29_ENET_RD0
AG28_ENET_RD1
AF29_ENET_RD2
AF28_ENET_RD3
AC18_SPDIF_EXT_CLK
AD18_SPDIF_RX
AE18_SPDIF_TX
AD20_ECSPI1_MISO
AE20_ECSPI1_SS0
AF20_ECSPI1_SCLK
AC20_ECSPI1_MOSI
AH21_ECSPI2_SCLK
AJ22_ECSPI2_SS0
AJ21_ECSPI2_MOSI
AH20_ECSPI2_MISO
AA26_SD2_DATA2
AA25_SD2_DATA3
AB28_SD2_CMD
AB29_SD2_CLK
AC28_SD2_DATA0
AC29_SD2_DATA1
AD28_SD2_RESET_B
AD29_SD2_nCD
AC26_SD2_WP
U26_SD1_DATA4
AA29_SD1_DATA5
AA28_SD1_DATA6
U25_SD1_DATA7
W26_SD1_STROBE
W25_SD1_RESET_B
V29_SD1_DATA2
V28_SD1_DATA3
W29_SD1_CMD
W28_SD1_CLK
Y29_SD1_DATA0
Y28_SD1_DATA1
GND
GND



2.5.2 SoM FETMX8MPQ-C Pin Details

Table 1 LEFT_UP (P1) connector pins (odd)

Num	Ball	Signal	GPIO	Vol	Spec.	Default
LU_1	—	GND	—	—	GND	GND
LU_3	AH4	UART2_TXD	GPIO5_IO25	3.3V	UART2(A53 debug) data sending	UART2_TXD
LU_5	AF6	UART2_RXD	GPIO5_IO24	3.3V	UART2(A53 debug) data receiving	UART2_RXD
LU_7	AE6	UART3_RXD	GPIO5_IO26	3.3V	UART3 data receiving	UART1_CTS
LU_9	AJ4	UART3_TXD	GPIO5_IO27	3.3V	UART3 data sending	UART1_RTS
LU_11	AF8	I2C4_SCL	GPIO5_IO20	3.3V	I2C4 clock	I2C4_SCL
LU_13	AD8	I2C4_SDA	GPIO5_IO21	3.3V	I2C4 data	I2C4_SDA
LU_15	—	GND	—	—	GND	GND
LU_17	AH6	I2C2_SCL	GPIO5_IO16	3.3V	I2C2 clock	I2C2_SCL
LU_19	AE8	I2C2_SDA	GPIO5_IO17	3.3V	I2C2 data	I2C2_SDA
LU_21	AJ6	I2C3_SDA	GPIO5_IO19	3.3V	I2C3 data	I2C3_SDA
LU_23	AJ7	I2C3_SCL	GPIO5_IO18	3.3V	I2C3 clock	I2C3_SCL
LU_25	—	GND	—	—	GND	GND
LU_27	AH8	SAI1_RXC	GPIO4_IO1	1.8V	SAI1 receive bit clock	4G_RST
LU_29	AF10	SAI1_RXD1	GPIO4_IO3	1.8V	SAI1 receive data 1	5GPWR_RESE
LU_31	AC10	SAI1_RXD0	GPIO4_IO2	1.8V	SAI1 receive data 0	5GPWR_ON/O
LU_33	AJ9	SAI1_RXFS	GPIO4_IO0	1.8V	SAI1 receive frame sync	4G/5G_PWR
LU_35	—	GND	—	—	GND	GND
LU_37	AH9	SAI1_RXD2	GPIO4_IO4	1.8V	SAI1 receive data 2	ENET1_MDC

LU_39	AJ8	SAI1_RXD3	GPIO4_IO5	1.8V	SAI1 receivedata 3	ENET1_MDIO
LU_41	AD12	SAI1_TXD3	GPIO4_IO15	1.8V	SAI1 send data 3	ENET1_TD3
LU_43	AH11	SAI1_TXD2	GPIO4_IO14	1.8V	SAI1 send data 2	ENET1_TD2
LU_45	AJ10	SAI1_TXD1	GPIO4_IO13	1.8V	SAI1 send data 1	ENET1_TD1
LU_47	AJ11	SAI1_TXD0	GPIO4_IO12	1.8V	SAI1 send data 0	ENET1_TD0
LU_49	—	GND	—	—	GND	GND
LU_51	AH14	SAI1_TXD5	GPIO4_IO17	1.8V	SAI1 send data 5	ENET1_TXC
LU_53	AH13	SAI1_TXD4	GPIO4_IO16	1.8V	SAI1 send data 4	ENET1_TX_CT
LU_55	—	GND	—	—	GND	GND
LU_57	AJ12	SAI1_TXC	GPIO4_IO11	1.8V	SAI1 send bit clock	ENET1_RXC
LU_59	AF12	SAI1_TXFS	GPIO4_IO10	1.8V	SAI1 send frame sync	ENET1_RX_C
LU_61	—	GND	—	—	GND	GND
LU_63	AD10	SAI1_RXD4	GPIO4_IO6	1.8V	SAI1 receive data 4	ENET1_RD0
LU_65	AE10	SAI1_RXD5	GPIO4_IO7	1.8V	SAI1 receive data 5	ENET1_RD1
LU_67	AH10	SAI1_RXD6	GPIO4_IO8	1.8V	SAI1 receive data 6	ENET1_RD2
LU_69	AH12	SAI1_RXD7	GPIO4_IO9	1.8V	SAI1 receive data 7	ENET1_RD3
LU_71	—	GND	—	—	GND	GND
LU_73	AC12	SAI1_TXD6	GPIO4_IO18	1.8V	SAI1 send data 6	GPIO_KEY2
LU_75	AJ13	SAI1_TXD7	GPIO4_IO19	1.8V	SAI1 send data 7	CC_nINT
LU_77	AE12	SAI1_MCLK	GPIO4_IO20	1.8V	SAI1 main clock	USB1_SS_SEL
LU_79	—	GND	—	—	GND	GND

Table 2 LEFT_UP (P1) connector pins (even)

Num	Ball	Signal	GPIO	Vol	Spec.	Default function
LU_2	—	GND	—	—	GND	GND
LU_4	AJ3	UART1_TXD	GPIO5_IO23	3.3V	UART1 data sending	UART1_TXD
LU_6	AD6	UART1_RXD	GPIO5_IO22	3.3V	UART1 data receiving	UART1_RXD
LU_8	—	GND	—	—	GND	GND
LU_10	AH5	UART4_TXD	GPIO5_IO29	3.3V	UART4 (M7 debug)data	UART4_TXD
LU_12	AJ5	UART4_RXD	GPIO5_IO28	3.3V	UART4 (M7 debug)data	UART4_RXD
LU_14	—	GND	—	—	GND	GND
LU_16	AC14	SAI5_RXFS	GPIO3_IO19	1.8V	SAI5 receive frame sync	CSI_P2_RESET
LU_18	AD14	SAI5_RXC	GPIO3_IO20	1.8V	SAI5 receive bit clock	CSI_P2_PWDN
LU_20	AF16	SAI5_RXD2	GPIO3_IO23	1.8V	SAI5 receive data 2	HOST_WL_WA
LU_22	AD16	SAI5_RXD1	GPIO3_IO22	1.8V	SAI5 receive data 1	PCM_SYNC
LU_24	AE14	SAI5_RXD3	GPIO3_IO24	1.8V	SAI5 receive data 3	PCM_OUT
LU_26	AF14	SAI5_MCLK	GPIO3_IO25	1.8V	SAI5 main clock	PCM_CLK
LU_28	AE16	SAI5_RXD0	GPIO3_IO21	1.8V	SAI5 receive data 0	PCM_IN
LU_30	—	GND	—	—	GND	GND
LU_32	AJ16	SAI2_RXC	GPIO4_IO22	3.3V	SAI2 receive bit clock	CAN1_TX
LU_34	AH15	SAI2_TXC	GPIO4_IO25	3.3V	SAI2 send bit clock	CAN1_RX
LU_36	AH17	SAI2_RXFS	GPIO4_IO21	3.3V	SAI2 receive frame sync	SPI_INT
LU_38	AJ17	SAI2_TXFS	GPIO4_IO24	3.3V	SAI2 send frame sync	GPIO_KEY1
LU_40	AH16	SAI2_TXD	GPIO4_IO26	3.3V	SAI2 send data	CAN2_TX
LU_42	AJ15	SAI2_MCLK	GPIO4_IO27	3.3V	SAI2 main clock	CAN2_RX
LU_44	AJ14	SAI2_RXD	GPIO4_IO23	3.3V	SAI2 receive data	USB_HUB_RST
LU_46	—	GND	—	—	GND	GND
LU_48	AJ18	SAI3_RXC	GPIO4_IO29	3.3V	SAI3 receive bit clock	CODEC_PWRE
LU_50	AJ19	SAI3_RXFS	GPIO4_IO28	3.3V	SAI3 receive frame sync	AUD_nINT

LU_52	AJ20	SAI3_MCLK	GPIO5_IO2	3.3V	SAI3 main clock	SAI3_MCLK
LU_54	—	GND	—	—	GND	GND
LU_56	AH19	SAI3_TXC	GPIO5_IO0	3.3V	SAI3 send bit clock	SAI3_TXC
LU_58	AC16	SAI3_TXFS	GPIO4_IO31	3.3V	SAI3 send frame sync	SAI3_TXFS
LU_60	AH18	SAI3_TXD	GPIO5_IO1	3.3V	SAI3 send data	SAI3_TXD
LU_62	AF18	SAI3_RXD	GPIO4_IO30	3.3V	SAI3 receive data	SAI3_RXD
LU_64	—	GND	—	—	GND	GND
LU_66	K28	CLKIN1	—	3.3V	CLK input 1	CLKIN1
LU_68	—	GND	—	—	GND	GND
LU_70	K29	CLKOUT1	—	3.3V	CLK output 1	CLKOUT1
LU_72	—	GND	—	—	GND	GND
LU_74	L28	CLKIN2	—	3.3V	CLK input 2	CLKIN2
LU_76	—	GND	—	—	GND	GND
LU_78	L29	CLKOUT2	—	3.3V	CLK output 2	CLKOUT2
LU_80	—	GND	—	—	GND	GND

Table 3 RIGHT_UP （P2 ） pins (odd)

Num	Ball	Signal	GPIO	Vol	Spec.	Default function
RU_1	—	GND	—	—	GND	GND
RU_3	D10	USB1_DP	—	—	USB1 data+	USB1_DP
RU_5	E10	USB1_DN	—	—	USB1 data-	USB1_DN
RU_7	—	GND	—	—	GND	GND
RU_9	A11	USB1_VBUS_3	—	3.3V	USB1_VBUS detect	USB1_VBUS_3
RU_11	D12	USB2_VBUS_3	—	3.3V	USB2_VBUS detect	USB2_VBUS_3
RU_13	—	GND	—	—	GND	GND
RU_15	A3	GPIO1_IO06	GPIO1_IO6	3.3V	GPIO	CSI1_nRST3.3
RU_17	B4	GPIO1_IO05	GPIO1_IO5	3.3V	GPIO	CSI1_SYNC3.3
RU_19	A4	GPIO1_IO14	GPIO1_IO14	3.3V	GPIO	TYPEC_HOST_
RU_21	B5	GPIO1_IO15	GPIO1_IO15	3.3V	GPIO	CSI_MCLK3.3
RU_23	A8	GPIO1_IO08	GPIO1_IO8	3.3V	GPIO	PCIE_RST
RU_25	A5	GPIO1_IO12	GPIO1_IO12	3.3V	GPIO	TP_INT
RU_27	B8	GPIO1_IO09	GPIO1_IO9	3.3V	GPIO	ACC_INT
RU_29	A7	GPIO1_IO00	GPIO1_IO0	3.3V	GPIO	LVDS_CTP_INT
RU_31	—	GND	—	—	GND	GND
RU_33	B7	GPIO1_IO10	GPIO1_IO10	3.3V	GPIO	LVDS_CTP_RS
RU_35	A6	GPIO1_IO13	GPIO1_IO13	3.3V	GPIO	LVDS_PWR_EN
RU_37	B6	WDOG_B	GPIO1_IO2	3.3V	watchdog	WDOG_B
RU_39	F6	GPIO1_IO07	GPIO1_IO7	3.3V	GPIO	DSI_EN
RU_41	D8	GPIO1_IO11	GPIO1_IO11	3.3V	GPIO	LVDS_PWM
RU_43	E8	GPIO1_IO01	GPIO1_IO1	3.3V	GPIO	DSI_BL_PWM
RU_45	—	GND	—	—	GND	GND
RU_47	G8	BOOT_MODE2	—	3.3V	BOOT booting mode select	BOOT_MODE2
RU_49	F8	BOOT_MODE1	—	3.3V	BOOT booting mode select	BOOT_MODE1
RU_51	G10	BOOT_MODE0	—	3.3V	BOOT booting mode select	BOOT_MODE0
RU_53	G12	BOOT_MODE3	—	3.3V	BOOT booting mode select	BOOT_MODE3
RU_55	—	GND	—	—	GND	GND
RU_57	G14	JTAG_TMS	—	3.3V	JTAG test mode select	JTAG_TMS
RU_59	F14	JTAG_TDO	—	3.3V	JTAG test data serial output	JTAG_TDO
RU_61	G16	JTAG_TDI	—	3.3V	JTAG test data serial input	JTAG_TDI
RU_63	G18	JTAG_TCK	—	3.3V	JTAG detect clock	JTAG_TCK

RU_65	G20	JTAG_MOD	—	3.3V	JTAG mode select	JTAG_MOD
RU_67	—	GND	—	—	GND	GND
RU_69	J29	POR_B	—	1.8V	CPU reset	POR_B
RU_71	F22	PMIC_ON_REQ	—	1.8V	PMIC power supply request	PMIC_ON_REQ
RU_73	G22	ONOFF	—	1.8V	power on/ off signal	ONOFF
RU_75	R26	NAND_DQS	GPIO3_IO14	1.8V	NAND_DQS clock	NAND_DQS Do not used for carrier board
RU_77	—	SYS_NRST	—	1.8V	SoM power reset	SYS_NRST
RU_79	—	GND	—	—	GND	GND

Table 4 RIGHT (P2) (even)

Num	Ball	Signal	GPIO	Vol	Spec.	Default function
RU_2	—	GND	—	—	GND	GND
RU_4	B9	USB1_RXN	—	—	USB1 receive-	USB1_RXN
RU_6	A9	USB1_RXP	—	—	USB1 receive+	USB1_RXP
RU_8	—	GND	—	—	GND	GND
RU_10	B10	USB1_TXN	—	—	USB1 send-	USB1_TXN
RU_12	A10	USB1_TXP	—	—	USB1 send+	USB1_TXP
RU_14	—	GND	—	—	GND	GND
RU_16	B12	USB2_RXN	—	—	USB2 receive-	USB2_RXN
RU_18	A12	USB2_RXP	—	—	USB2 receive+	USB2_RXP
RU_20	—	GND	—	—	GND	GND
RU_22	D14	USB2_DP	—	—	USB2 data+	USB2_DP
RU_24	E14	USB2_DN	—	—	USB2 data-	USB2_DN
RU_26	—	GND	—	—	GND	GND
RU_28	B13	USB2_TXN	—	—	USB2 send-	USB2_TXN
RU_30	A13	USB2_TXP	—	—	USB2 send+	USB2_TXP
RU_32	—	GND	—	—	GND	GND
RU_34	B14	PCIE_RXN	—	—	PCIE data receive-	PCIE_RXN
RU_36	A14	PCIE_RXP	—	—	PCIE data receive+	PCIE_RXP
RU_38	—	GND	—	—	GND	GND
RU_40	B15	PCIE_TXN	—	—	PCIE data send-	PCIE_TXN
RU_42	A15	PCIE_TXP	—	—	PCIE data send+	PCIE_TXP
RU_44	—	GND	—	—	GND	GND
RU_46	D16	PCIE_CLKP	—	—	PCIE clock input+	PCIE_CLKP
RU_48	E16	PCIE_CLKN	—	—	PCIE clock input-	PCIE_CLKN
RU_50	—	GND	—	—	GND	GND
RU_52	B16	DSI_DN0	—	—	DSI data 0-	DSI_DN0
RU_54	A16	DSI_DP0	—	—	DSI data 0+	DSI_DP0
RU_56	—	GND	—	—	GND	GND
RU_58	B17	DSI_DN1	—	—	DSI data 1-	DSI_DN1
RU_60	A17	DSI_DP1	—	—	DSI data 1+	DSI_DP1
RU_62	—	GND	—	—	GND	GND
RU_64	B18	DSI_CKN	—	—	DSI clock -	DSI_CKN
RU_66	A18	DSI_CKP	—	—	DSI clock +	DSI_CKP
RU_68	—	GND	—	—	GND	GND
RU_70	B19	DSI_DN2	—	—	DSI data 2-	DSI_DN2
RU_72	A19	DSI_DP2	—	—	DSI data 2+	DSI_DP2
RU_74	—	GND	—	—	GND	GND
RU_76	B20	DSI_DN3	—	—	DSI data 3-	DSI_DN3

RU_78	A20	DSI_DP3	—	—	DSI data 3+	DSI_DP3
RU_80	—	GND	—	—	GND	GND

Table 5 LEFT_DOWN (P3) (odd)

Num	Ball	Signal	GPIO	Vol	Spec.	Default function
LD_1	—	GND	—	—	GND	GND
LD_3	AE22	HDMI_HPD	GPIO3_IO29	3.3V	HDMI hot plug detect	HDMI_HPD
LD_5	AF22	HDMI_DDC_SDA	GPIO3_IO27	3.3V	HDMI_DDC data	HDMI_DDC_SD
LD_7	—	GND	—	—	GND	GND
LD_9	AC22	HDMI_DDC_SCL	GPIO3_IO26	3.3V	HDMI_DDC clock	HDMI_DDC_SC
LD_11	AD22	HDMI_CEC	GPIO3_IO28	3.3V	HDMI_CEC recognize	HDMI_CEC
LD_13	—	GND	—	—	GND	GND
LD_15	AH22	EARC_N_HPD	—	—	eARC differential -	EARC_N_HPD
LD_17	AJ23	EARC_P_UTIL	—	—	eARC differential +	EARC_P_UTIL
LD_19	—	GND	—	—	GND	GND
LD_21	AJ24	HDMI_TXCN	—	—	HDMI differential clock-	HDMI_TXCN
LD_23	AH24	HDMI_TXCP	—	—	HDMI differential clock+	HDMI_TXCP
LD_25	—	GND	—	—	GND	GND
LD_27	AJ25	HDMI_TXN0	—	—	HDMI differential data 0-	HDMI_TXN0
LD_29	AH25	HDMI_TXP0	—	—	HDMI differential data 0+	HDMI_TXP0
LD_31	—	GND	—	—	GND	GND
LD_33	AJ26	HDMI_TXN1	—	—	HDMI differential data 1-	HDMI_TXN1
LD_35	AH26	HDMI_TXP1	—	—	HDMI differential data 1+	HDMI_TXP1
LD_37	—	GND	—	—	GND	GND
LD_39	AJ27	HDMI_TXN2	—	—	HDMI differential data 2-	HDMI_TXN2
LD_41	AH27	HDMI_TXP2	—	—	HDMI differential data 2+	HDMI_TXP2
LD_43	—	GND	—	—	GND	GND
LD_45	AH28	ENET_MDC	GPIO1_IO16	1.8V	ENET serial management clock	ENET_MDC
LD_47	AH29	ENET_MDIO	GPIO1_IO17	1.8V	ENET serial management data	ENET_MDIO
LD_49	AD24	ENET_TD3	GPIO1_IO18	1.8V	RGMII data send 3	ENET_TD3
LD_51	AF26	ENET_TD2	GPIO1_IO19	1.8V	RGMII data send 2	ENET_TD2
LD_53	AE26	ENET_TD1	GPIO1_IO20	1.8V	RGMII data send 1	ENET_TD1
LD_55	AC25	ENET_TD0	GPIO1_IO21	1.8V	RGMII data send 0	ENET_TD0
LD_57	—	GND	—	—	GND	GND
LD_59	AE24	ENET_TXC	GPIO1_IO23	1.8V	RGMII send clock	ENET_TXC
LD_61	AF24	ENET_TX_CTL	GPIO1_IO22	1.8V	RGMII send control	ENET_TX_CTL
LD_63	—	GND	—	—	GND	GND
LD_65	AE29	ENET_RXC	GPIO1_IO25	1.8V	RGMII receive clock	ENET_RXC
LD_67	AE28	ENET_RX_CTL	GPIO1_IO24	1.8V	RGMII receive control	ENET_RX_CTL
LD_69	—	GND	—	—	GND	GND
LD_71	AG29	ENET_RD0	GPIO1_IO26	1.8V	RGMII receive data 0	ENET_RD0
LD_73	AG28	ENET_RD1	GPIO1_IO27	1.8V	RGMII receive data 1	ENET_RD1
LD_75	AF29	ENET_RD2	GPIO1_IO28	1.8V	RGMII receive data 2	ENET_RD2
LD_77	AF28	ENET_RD3	GPIO1_IO29	1.8V	RGMII receive data 3	ENET_RD3
LD_79	—	GND	—	—	GND	GND

Table 6 LEFT_DOWN (P3) (even)

Num	Ball	Signal	GPIO	Vol	Spec.	Default function
LD_2	—	GND	—	—	GND	GND
LD_4	AC18	SPDIF_EXT_CL	GPIO5_IO5	3.3V	SPDIF clock	ENET_nRST
LD_6	AD18	SPDIF_RX	GPIO5_IO4	3.3V	SPDIF receive	ENET1_nRST
LD_8	AE18	SPDIF_TX	GPIO5_IO3	3.3V	SPDIF send	ENET_nINT
LD_10	—	GND	—	—	GND	GND
LD_12	AD20	ECSPI1_MISO	GPIO5_IO8	3.3V	ECSPI1 host input slave output	GPIO_LED1
LD_14	AE20	ECSPI1_SS0	GPIO5_IO9	3.3V	ECSPI1 chip select	GPIO_LED2
LD_16	AF20	ECSPI1_SCLK	GPIO5_IO6	3.3V	ECSPI1 clock	UART3_RXD
LD_18	AC20	ECSPI1_MOSI	GPIO5_IO7	3.3V	ECSPI1 host output slave input	UART3_TXD
LD_20	—	GND	—	—	GND	GND
LD_22	AH21	ECSPI2_SCLK	GPIO5_IO10	3.3V	ECSPI2 clock	ECSPI2_SCLK
LD_24	AJ22	ECSPI2_SS0	GPIO5_IO13	3.3V	ECSPI2 chip select	ECSPI2_SS0
LD_26	AJ21	ECSPI2_MOSI	GPIO5_IO11	3.3V	ECSPI2 host output slave input	ECSPI2_MOSI
LD_28	AH20	ECSPI2_MISO	GPIO5_IO12	3.3V	ECSPI2 host input slave output	ECSPI2_MISO
LD_30	—	GND	—	—	GND	GND
LD_32	AA26	SD2_DATA2	GPIO2_IO17	1.8/3.3	SD2 data bit 2	SD2_DATA2
LD_34	AA25	SD2_DATA3	GPIO2_IO18	1.8/3.3	SD2 data bit 3	SD2_DATA3
LD_36	AB28	SD2_CMD	GPIO2_IO14	1.8/3.3	SD2 command signal	SD2_CMD
LD_38	AB29	SD2_CLK	GPIO2_IO13	1.8/3.3	SD2 clock	SD2_CLK
LD_40	AC28	SD2_DATA0	GPIO2_IO15	1.8/3.3	SD2 data bit 0	SD2_DATA0
LD_42	AC29	SD2_DATA1	GPIO2_IO16	1.8/3.3	SD2 data bit 1	SD2_DATA1
LD_44	AD28	SD2_RESET_B	GPIO2_IO19	1.8/3.3	SD2 reset signal	Carrier board not use
LD_46	AD29	SD2_NCD	GPIO2_IO12	1.8/3.3	SD2 card detect signal	SD2_nCD
LD_48	AC26	SD2_WP	GPIO2_IO20	1.8/3.3	SD2 write protect signal	TYPEC_EN_B
LD_50	—	GND	—	—	GND	GND
LD_52	U26	SD1_DATA4	GPIO2_IO6	1.8V	SD1 data bit 4	BT_HOST_WAKE
LD_54	AA29	SD1_DATA5	GPIO2_IO7	1.8V	SD1 data bit 5	BT_WAKE_B
LD_56	AA28	SD1_DATA6	GPIO2_IO8	1.8V	SD1 data bit 6	WIFI_REG_ON
LD_58	U25	SD1_DATA7	GPIO2_IO9	1.8V	SD1 data bit 7	WIFI_HOST_WAK
LD_60	—	GND	—	—	GND	GND
LD_62	W26	SD1_STROBE	GPIO2_IO11	1.8V	SD1 strobe signal	CSI1_PWDN
LD_64	W25	SD1_RESET_B	GPIO2_IO10	1.8V	SD1 reset signal	BT_REG_ON
LD_66	V29	SD1_DATA2	GPIO2_IO4	1.8V	SD1 data bit 2	SD1_DATA2
LD_68	V28	SD1_DATA3	GPIO2_IO5	1.8V	SD1 data bit 3	SD1_DATA3
LD_70	W29	SD1_CMD	GPIO2_IO1	1.8V	SD1 command signal	SD1_CMD
LD_72	—	GND	—	—	GND	GND
LD_74	W28	SD1_CLK	GPIO2_IO0	1.8V	SD1 clock	SD1_CLK
LD_76	Y29	SD1_DATA0	GPIO2_IO2	1.8V	SD1 data bit 0	SD1_DATA0
LD_78	Y28	SD1_DATA1	GPIO2_IO3	1.8V	SD1 data bit 1	SD1_DATA1
LD_80	—	GND	—	—	GND	GND

Table 7 RIGHT_DOWN (P4) (odd)

Num	Ball	Signal	GPIO	Vol	Spec.	Default function
RD_1	—	GND	—	—	GN	GND
RD_3	D22	CSI1_CKP	—	—	CSI1 clock+	CSI1_CKP
RD_5	E22	CSI1_CKN	—	—	CSI1 clock-	CSI1_CKN
RD_7	—	GND	—	—	GN	GND
RD_9	E18	CSI1_DN0	—	—	CSI1 data 0-	CSI1_DN0
RD_11	D18	CSI1_DP0	—	—	CSI1 data 0+	CSI1_DP0
RD_13	—	GND	—	—	GN	GND
RD_15	E20	CSI1_DN1	—	—	CSI1 data 1-	CSI1_DN1
RD_17	D20	CSI1_DP1	—	—	CSI1 data 1+	CSI1_DP1
RD_19	—	GND	—	—	GN	GND
RD_21	E24	CSI1_DN2	—	—	CSI1 data 2-	CSI1_DN2
RD_23	D24	CSI1_DP2	—	—	CSI1 data 2+	CSI1_DP2
RD_25	—	GND	—	—	GN	GND
RD_27	E26	CSI1_DN3	—	—	CSI1 data 3-	CSI1_DN3
RD_29	D26	CSI1_DP3	—	—	CSI1 data 3+	CSI1_DP3
RD_31	—	GND	—	—	GN	GND
RD_33	B21	CSI2_DN3	—	—	CSI2 data 3-	CSI2_DN3
RD_35	A21	CSI2_DP3	—	—	CSI2 data 3+	CSI2_DP3
RD_37	—	GND	—	—	GN	GND
RD_39	B22	CSI2_DN2	—	—	CSI2 data 2-	CSI2_DN2
RD_41	A22	CSI2_DP2	—	—	CSI2 data 2+	CSI2_DP2
RD_43	—	GND	—	—	GN	GND
RD_45	B24	CSI2_DN1	—	—	CSI2 data 1-	CSI2_DN1
RD_47	A24	CSI2_DP1	—	—	CSI2 data 1+	CSI2_DP1
RD_49	—	GND	—	—	GN	GND
RD_51	B25	CSI2_DN0	—	—	CSI2 data 0-	CSI2_DN0
RD_53	A25	CSI2_DP0	—	—	CSI2 data 0+	CSI2_DP0
RD_55	—	GND	—	—	GN	GND
RD_57	B23	CSI2_CKN	—	—	CSI2 clock-	CSI2_CKN
RD_59	A23	CSI2_CKP	—	—	CSI2 clock+	CSI2_CKP
RD_61	—	GND	—	—	GN	GND
RD_63	—	NVCC_SNVS_1	—	1.8V	SoM SNVS voltage	NVCC_SNVS_1
RD_65	—	GND	—	—	GN	GND
RD_67	—	GND	—	—	GN	GND
RD_69	—	GND	—	—	GN	GND
RD_71	—	GND	—	—	GN	GND
RD_73	—	VSYS_5V	—	5V	SoM main power input 5V	VSYS_5V
RD_75	—	VSYS_5V	—	5V	SoM main power input 5V	VSYS_5V
RD_77	—	VSYS_5V	—	5V	SoM main power input 5V	VSYS_5V
RD_79	—	VSYS_5V	—	5V	SoM main power input 5V	VSYS_5V

Table 8 RIGHT_DOWN (P4) (even)

Num	Ball	Signal	GPIO	Vol	Spec.	Default function
RD_2	—	GN	—	—	GND	GND
RD_4	C29	LVDS1_TX3_P	—	—	LVDS1 data 3+	LVDS1_TX3
RD_6	D28	LVDS1_TX3_N	—	—	LVDS1 data 3-	LVDS1_TX3
RD_8	—	GN	—	—	GND	GND
RD_10	A28	LVDS1_CLK_P	—	—	LVDS1 clock+	LVDS1_CLK
RD_12	B28	LVDS1_CLK_N	—	—	LVDS1 clock-	LVDS1_CLK
RD_14	—	GN	—	—	GND	GND
RD_16	B29	LVDS1_TX2_P	—	—	LVDS1 data 2+	LVDS1_TX2
RD_18	C28	LVDS1_TX2_N	—	—	LVDS1 data 2-	LVDS1_TX2
RD_20	—	GN	—	—	GND	GND
RD_22	A27	LVDS1_TX1_P	—	—	LVDS1 data 1+	LVDS1_TX1
RD_24	B27	LVDS1_TX1_N	—	—	LVDS1 data 1-	LVDS1_TX1
RD_26	—	GN	—	—	GND	GND
RD_28	A26	LVDS1_TX0_P	—	—	LVDS1 data 0+	LVDS1_TX0
RD_30	B26	LVDS1_TX0_N	—	—	LVDS1 data 0-	LVDS1_TX0
RD_32	—	GN	—	—	GND	GND
RD_34	H29	LVDS0_TX3_P	—	—	LVDS0 data 3+	LVDS0_TX3
RD_36	J28	LVDS0_TX3_N	—	—	LVDS0 data 3-	LVDS0_TX3
RD_38	—	GN	—	—	GND	GND
RD_40	D29	LVDS0_CLK_P	—	—	LVDS0 clock+	LVDS0_CLK
RD_42	G28	LVDS0_CLK_N	—	—	LVDS0 clock-	LVDS0_CLK
RD_44	—	GN	—	—	GND	GND
RD_46	G29	LVDS0_TX2_P	—	—	LVDS0 data 2+	LVDS0_TX2
RD_48	H28	LVDS0_TX2_N	—	—	LVDS0 data 2-	LVDS0_TX2
RD_50	—	GN	—	—	GND	GND
RD_52	E29	LVDS0_TX1_P	—	—	LVDS0 data 1+	LVDS0_TX1
RD_54	F28	LVDS0_TX1_N	—	—	LVDS0 data 1-	LVDS0_TX1
RD_56	—	GN	—	—	GND	GND
RD_58	D29	LVDS0_TX0_P	—	—	LVDS0 data 0+	LVDS0_TX0
RD_60	E28	LVDS0_TX0_N	—	—	LVDS0 data 0-	LVDS0_TX0
RD_62	—	GN	—	—	GND	GND
RD_64	—	GN	—	—	GND	GND
RD_66	—	VSD_3V3	—	3.3V	SD card power supply	VSD_3V3
RD_68	—	VSD_3V3	—	3.3V	SD card power supply	VSD_3V3
RD_70	—	GN	—	—	GND	GND
RD_72	—	GN	—	—	GND	GND
RD_74	—	VDD_3V3	—	3.3V	SoM powered done	VDD_3V3
RD_76	—	VSYS_5V	—	5V	SoM main power input 5V	VSYS_5V
RD_78	—	VSYS_5V	—	5V	SoM main power input 5V	VSYS_5V
RD_80	—	VSYS_5V	—	5V	SoM main power input 5V	VSYS_5V

2.6 SoM FETMX8MM-C Pin Spec.

2.6.1 Power Pins

Pin	Signal	I/ O	Default function	Pin NO.
Power	VSYS_5V	Power input	Som power supplying pin, 5V	RD_73
				RD_75
				RD_77
				RD_79
				RD_76
				RD_78
				RD_80
	VSD_3V3	Power output	Carrier board SD card power supply, 3.3V	RD_66
				RD_68
	VSD_3V3	Power output	SoM powered done, used for carrier board powering sequence control, can not be used for carrier board power supply	RD_74
	NVCC_SNVS_1V8	Power input	SoM SNVS voltage, if no special requirement, please suspend it	RD_63
	GND		SoM power ground, all GND pins should be circuited	-

2.6.2 Reset Control Pin

Pin	Signal	I/ O	Default function	Pin NO.
SoM reset	SYS_nRST	I	SoM power off and reset, low voltage valid	RU_77
CPU reset	POR_B	I	CPU reset pin	RU_69

2.6.3 Boot Pin

Pin	Signal	I/ O	Default function	Pin NO.
Booting mode selection	BOOT_MODE0	I	BOOT device select	RU_51
	BOOT_MODE1	I		RU_49
	BOOT_MODE2	I		RU_47
	BOOT_MODE3	I		RU_53

2.6.4 Function Control Pin

Pin	Signal	I/ O	Default function	Pin NO.
Functional control	ONOFF	I	SoM power pin, could be suspended if not needed	RU_73
	VDD_3V3	O	SoM output to control carrier board power sequence	RD_74
	PMIC_ON_REQ	O	SoM PMIC power request signal, no special requirement, please suspend it	RU_71

2.6.5 USB

Peripheral	Signal	I/O	Default function	Pin No.
USB1	USB1_VBUS_3V3	I	USB1_VBUS detect	RU_9
	USB1_DP	I/O	USB1 data+	RU_3
	USB1_DN	I/O	USB1 data-	RU_5
	USB1_RXN	I	USB1 receive-	RU_4
	USB1_RXP	I	USB1 receive+	RU_6
	USB1_TXN	O	USB1 send-	RU_10
	USB1_TXP	O	USB1 send+	RU_12
USB2	USB2_VBUS_3V3	I	USB2_VBUS detect	RU_11
	USB2_RXN	I	USB2 receive-	RU_16
	USB2_RXP	I	USB2 receive+	RU_18
	USB2_DP	I/O	USB2 data+	RU_22
	USB2_DN	I/O	USB2 data-	RU_24
	USB2_TXN	O	USB2 send-	RU_28
	USB2_TXP	O	USB2 send+	RU_30

2.6.6 SPI

Peripheral	Signal	I/O	Default function	Pin No.
SPI0	ECSPI1_MISO	I	ECSPI1 host input slave output	LD_12
	ECSPI1_SS0	O	ECSPI1 chip select	LD_14
	ECSPI1_SCLK	O	ECSPI1 clock	LD_16
	ECSPI1_MOSI	O	ECSPI1 host output slave input	LD_18
SPI2	ECSPI2_SCLK	O	ECSPI2 clock	LD_22
	ECSPI2_SS0	O	ECSPI2 chip select	LD_24
	ECSPI2_MOSI	O	ECSPI2 host output slave input	LD_26
	ECSPI2_MISO	I	ECSPI2 host input slave output	LD_28

2.6.7 SAI

Peripheral	Signal	I/O	Default function	Pin No.
SAI1	SAI1_RXC	I	SAI1 receiving bit clock	LU_27
	SAI1_RXD1	I	SAI1 receive data 1	LU_29
	SAI1_RXD0	I	SAI1 receive data 0	LU_31
	SAI1_RXFS	I	SAI1 receive frame sync	LU_33
	SAI1_RXD2	I	SAI1 receive data 2	LU_37
	SAI1_RXD3	I	SAI1 receive data 3	LU_39
	SAI1_TXD3	O	SAI1 send data 3	LU_41
	SAI1_TXD2	O	SAI1 send data 2	LU_43
	SAI1_TXD1	O	SAI1 send data 1	LU_45
	SAI1_TXD0	O	SAI1 send data 0	LU_47
	SAI1_TXD5	O	SAI1 send data 5	LU_51
	SAI1_TXD4	O	SAI1 send data 4	LU_53
	SAI1_TXC	O	SAI1 send bit clock	LU_57
	SAI1_TXFS	O	SAI1 send frame sync	LU_59
	SAI1_RXD4	I	SAI1 receive data 4	LU_63

	SAI1_RXD5	I	SAI1 receive data 5	LU_65
	SAI1_RXD6	I	SAI1 receive data 6	LU_67
	SAI1_RXD7	I	SAI1 receive data 7	LU_69
	SAI1_TXD6	O	SAI1 send data 6	LU_73
	SAI1_TXD7	O	SAI1 send data 7	LU_75
	SAI1_MCLK	O	SAI1 main clock	LU_77
SAI2	SAI2_RXC	I	SAI2 receive bit clock	LU_32
	SAI2_TXC	O	SAI2 send bit clock	LU_34
	SAI2_RXFS	I	SAI2 receive frame sync	LU_36
	SAI2_TXFS	O	SAI2 send frame sync	LU_38
	SAI2_TXD	O	SAI2 send data	LU_40
	SAI2_MCLK	O	SAI2 main clock	LU_42
	SAI2_RXD	I	SAI2 receive data	LU_44
SAI3	SAI3_RXC	I	SAI3 receive bit clock	LU_48
	SAI3_RXFS	I	SAI3 receive frame sync	LU_50
	SAI3_MCLK	O	SAI3 main clock	LU_52
	SAI3_TXC	O	SAI3 send bit clock	LU_56
	SAI3_TXFS	O	SAI3 send frame sync	LU_58
	SAI3_TXD	O	SAI3 send data	LU_60
	SAI3_RXD	I	SAI3 receive data	LU_62
SAI5	SAI5_RXFS	I	SAI5 receive frame sync	LU_16
	SAI5_RXC	I	SAI5 receive bit clock	LU_18
	SAI5_RXD2	I	SAI5 receive data 2	LU_20
	SAI5_RXD1	I	SAI5 receive data 1	LU_22
	SAI5_RXD3	I	SAI5 receive data 3	LU_24
	SAI5_MCLK	O	SAI5 main clock	LU_26
	SAI5_RXD0	I	SAI5 receive data 0	LU_28

2.6.8 UART

Peripheral	Signal	I/O	Default function	Pin No.
UART1	UART1_TXD	O	UART1 data sending	LU_4
	UART1_RXD	I	UART1 data receiving	LU_6
UART2	UART2_TXD	O	UART2(A53 debug)data sending	LU_3
	UART2_RXD	I	UART2(A53 debug)data receiving	LU_5
UART3	UART3_RXD	I	UART3 data receiving	LU_7
	UART3_TXD	O	UART3 data sending	LU_9
UART4	UART4_TXD	O	UART4(M7 debug)data sending	LU_10
	UART4_RXD	I	UART4(M7 debug)data receiving	LU_12

2.6.9 IIC

Peripheral	Signal	I/O	Default function	Pin No.
I2C4	I2C4_SCL	O	I2C4 clock	LU_11
	I2C4_SDA	I/O	I2C4 data	LU_13
I2C2	I2C2_SCL	O	I2C2 clock	LU_17
	I2C2_SDA	I/O	I2C2 data	LU_19
I2C3	I2C3_SDA	I/O	I2C3 data	LU_21
	I2C3_SCL	O	I2C3 clock	LU_23

2.6.10 JTAG

Peripheral	Signal	I/O	Default function	Pin No.
JTAG	JTAG_TMS	I	JTAG test mode select	RU_57
	JTAG_TDO	O	JTAG test data serial output	RU_59
	JTAG_TDI	I	JTAG test data serial input	RU_61
	JTAG_TCK	I	JTAG detect clock	RU_63
	JTAG_MOD	I	JTAG mode select	RU_65

2.6.11 Ethernet

Peripheral	Signal	I/O	Default function	Pin No.
RGMII	ENET_MDC	O	ENET serial management clock	LD_45
	ENET_MDIO	I/O	ENET serial management data	LD_47
	ENET_TD3	O	RGMII data sending 3	LD_49
	ENET_TD2	O	RGMII data sending 2	LD_51
	ENET_TD1	O	RGMII data sending 1	LD_53
	ENET_TD0	O	RGMII data sending 0	LD_55
	ENET_TXC	O	RGMII send clock	LD_59
	ENET_TX_CTL	O	RGMII send control	LD_61
	ENET_RXC	I	RGMII receive clock	LD_65
	ENET_RX_CTL	I	RGMII receive control	LD_67
	ENET_RD0	I	RGMII receive data 0	LD_71
	ENET_RD1	I	RGMII receive data 1	LD_73
	ENET_RD2	I	RGMII receive data 2	LD_75
	ENET_RD3	I	RGMII receive data 3	LD_77
RGMII	ENET1_MDC	O	ENET serial management clock	LU_37
	ENET1_MDIO	I/O	ENET serial management data	LU_39
	ENET1_TD3	O	RGMII data sending 3	LU_41
	ENET1_TD2	O	RGMII data sending 2	LU_43
	ENET1_TD1	O	RGMII data sending 1	LU_45
	ENET1_TD0	O	RGMII data sending 0	LU_47
	ENET1_TXC	O	RGMII send clock	LU_51
	ENET1_TX_CTL	O	RGMII send control	LU_53
	ENET1_RXC	I	RGMII receive clock	LU_57
	ENET1_RX_CTL	I	RGMII receive control	LU_59
	ENET1_RD0	I	RGMII receive data 0	LU_63
	ENET1_RD1	I	RGMII receive data 1	LU_65
	ENET1_RD2	I	RGMII receive data 2	LU_67
	ENET1_RD3	I	RGMII receive data 3	LU_69

2.6.12 MIPI CSI

Peripheral	Signal	I/O	Default function	Pin No.
MIPI_CSI_P1	CSI1_CKP	I	CSI1 clock+	RD_3
	CSI1_CKN	I	CSI1 clock-	RD_5
	CSI1_DN0	I	CSI1 data 0-	RD_9
	CSI1_DP0	I	CSI1 data 0+	RD_11
	CSI1_DN1	I	CSI1 data 1-	RD_15
	CSI1_DP1	I	CSI1 data 1+	RD_17
	CSI1_DN2	I	CSI1 data 2-	RD_21
	CSI1_DP2	I	CSI1 data 2+	RD_23
	CSI1_DN3	I	CSI1 data 3-	RD_27
	CSI1_DP3	I	CSI1 data 3+	RD_29
MIPI_CSI_P2	CSI2_DN3	I	CSI2 data 3-	RD_33
	CSI2_DP3	I	CSI2 data 3+	RD_35
	CSI2_DN2	I	CSI2 data 2-	RD_39
	CSI2_DP2	I	CSI2 data 2+	RD_41
	CSI2_DN1	I	CSI2 data 1-	RD_45
	CSI2_DP1	I	CSI2 data 1+	RD_47
	CSI2_DN0	I	CSI2 data 0-	RD_51
	CSI2_DP0	I	CSI2 data 0+	RD_53
	CSI2_CKN	I	CSI2 clock-	RD_57
	CSI2_CKP	I	CSI2 clock+	RD_59

2.6.13 MIPI DSI

Peripheral	Signal	I/O	Default function	Pin No.
MIPI_DSI	DSI_DN0	O	DSI data 0-	RU_52
	DSI_DP0	O	DSI data 0+	RU_54
	DSI_DN1	O	DSI data 1-	RU_58
	DSI_DP1	O	DSI data 1+	RU_60
	DSI_CKN	O	DSI clock-	RU_64
	DSI_CKP	O	DSI clock+	RU_66
	DSI_DN2	O	DSI data 2-	RU_70
	DSI_DP2	O	DSI data 2+	RU_72
	DSI_DN3	O	DSI data 3-	RU_76
	DSI_DP3	O	DSI data 3+	RU_78

2.6.14 LVDS

Peripheral	Signal	I/O	Default function	Pin No.
LVDS1	LVDS1_TX3_P	O	LVDS1 data3+	RD_4
	LVDS1_TX3_N	O	LVDS1 data3-	RD_6
	LVDS1_CLK_P	O	LVDS1 clock+	RD_10
	LVDS1_CLK_N	O	LVDS1 clock-	RD_12
	LVDS1_TX2_P	O	LVDS1 data2+	RD_16
	LVDS1_TX2_N	O	LVDS1 data2-	RD_18
	LVDS1_TX1_P	O	LVDS1 data1+	RD_22
	LVDS1_TX1_N	O	LVDS1 data1-	RD_24
	LVDS1_TX0_P	O	LVDS1 data0+	RD_28
	LVDS1_TX0_N	O	LVDS1 data0-	RD_30
LVDS0	LVDS0_TX3_P	O	LVDS0 data3+	RD_34
	LVDS0_TX3_N	O	LVDS0 data3-	RD_36
	LVDS0_CLK_P	O	LVDS0 clock+	RD_40
	LVDS0_CLK_N	O	LVDS0 clock-	RD_42
	LVDS0_TX2_P	O	LVDS0 data2+	RD_46
	LVDS0_TX2_N	O	LVDS0 data2-	RD_48
	LVDS0_TX1_P	O	LVDS0 data1+	RD_52
	LVDS0_TX1_N	O	LVDS0 data1-	RD_54
	LVDS0_TX0_P	O	LVDS0 data0+	RD_58
	LVDS0_TX0_N	O	LVDS0 data0-	RD_60

2.6.15 PCIe

Peripheral	Signal	I/O	Default function	Pin No.
PCIE1	PCIE_RXN	I	PCIE data receiving-	RU_34
	PCIE_RXP	I	PCIE data receiving+	RU_36
	PCIE_TXN	O	PCIE data sending-	RU_40
	PCIE_TXP	O	PCIE data sending+	RU_42
	PCIE_CLKP	I	PCIE clock input+	RU_46
	PCIE_CLKN	I	PCIE clock input-	RU_48

2.6.16 HDMI

Peripheral	Signal	I/O	Default function	Pin No.
HDMI	HDMI_HPD	I	HDMI hot plug detect	LD_3
	HDMI_DDC_SDA	I/O	HDMI_DDC data	LD_5
	HDMI_DDC_SCL	O	HDMI_DDC clock	LD_9
	HDMI_CEC	I/O	HDMI_CEC detect	LD_11
	EARC_N_HPD	O	eARC differential-	LD_15
	EARC_P_UTIL	O	eARC differential+	LD_17
	HDMI_TXCN	O	HDMI differential clock-	LD_21
	HDMI_TXCP	O	HDMI differential clock+	LD_23
	HDMI_TXN0	O	HDMI differential data 0-	LD_27
	HDMI_TXP0	O	HDMI differential data 0+	LD_29
	HDMI_TXN1	O	HDMI differential data 1-	LD_33
	HDMI_TXP1	O	HDMI differential data 1+	LD_35
	HDMI_TXN2	O	HDMI differentialdata 2-	LD_39
	HDMI_TXP2	O	HDMI differentialdata 2+	LD_41

2.6.17 SD card slot

Peripheral	Signal	I/O	Default function	Pin No.
SD1	SD1_DATA4	I/O	SD1 data bit 4	LD_52
	SD1_DATA5	I/O	SD1 data bit 5	LD_54
	SD1_DATA6	I/O	SD1 data bit 6	LD_56
	SD1_DATA7	I/O	SD1 data bit 7	LD_58
	SD1_STROBE	I	SD1 strobe signal	LD_62
	SD1_RESET_B	O	SD1 reset signal	LD_64
	SD1_DATA2	I/O	SD1 data bit 2	LD_66
	SD1_DATA3	I/O	SD1 data bit 3	LD_68
	SD1_CMD	I/O	SD1 command signal	LD_70
	SD1_CLK	O	SD1 clock	LD_74
	SD1_DATA0	I/O	SD1 data bit 0	LD_76
	SD1_DATA1	I/O	SD1 data bit 1	LD_78
SD2	SD2_DATA2	I/O	SD2 data bit 2	LD_32
	SD2_DATA3	I/O	SD2 data bit 3	LD_34
	SD2_CMD	I/O	SD2 command signal	LD_36
	SD2_CLK	O	SD2 clock	LD_38
	SD2_DATA0	I/O	SD2 data bit 0	LD_40
	SD2_DATA1	I/O	SD2 data bit 1	LD_42
	SD2_RESET_B	O	SD2 reset signal	LD_44
	SD2_NCD	I	SD2 card detect signal	LD_46
	SD2_WP	I	SD2 write protect signal	LD_48

2.6.18 SPDIF

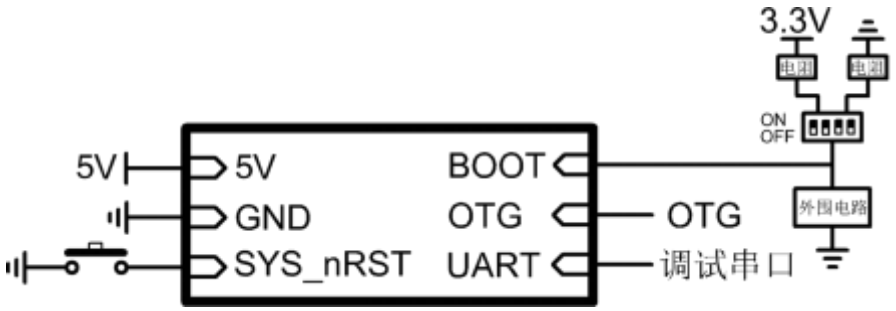
Peripheral	Signal	I/O	Default function	Pin No.
SPDIF	SPDIF_EXT_CLK	O	SPDIF clock	LD_4
	SPDIF_RX	I	SPDIF receive	LD_6
	SPDIF_TX	O	SPDIF send	LD_8

2.6.19 Clock input/ output

Peripheral	Signal	I/O	Default function	Pin No.
CLK	CLKIN1	I	CLK input 1	LU_66
	CLKOUT1	O	CLK output 1	LU_70
	CLKIN2	I	CLK input 2	LU_74
	CLKOUT2	O	CLK output 2	LU_78

2.7 SoM Designing Tips

The SoM FETMX8MPX-C is integrated with power, reset monitor circuit and storage circuit onto one compact module, 5V power input, reset and boot consist the minimum system



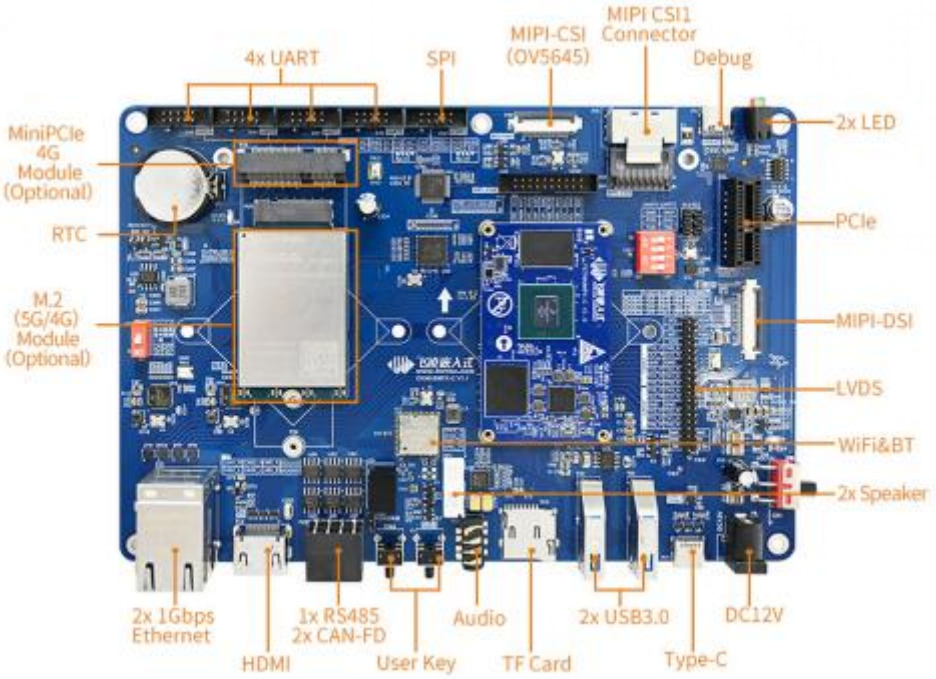
note: 电阻：resistor； 调试串口：serial debug port；外围电路：peripheral circuit

The minimum system schematic please refer to Appendix4, except minimum system, we kindly suggest users to mount some peripherals such as debug port to check serial output information, preserve OTG for firmware installation, and then refer to Forlinx SoM default definition to expand needed functions.

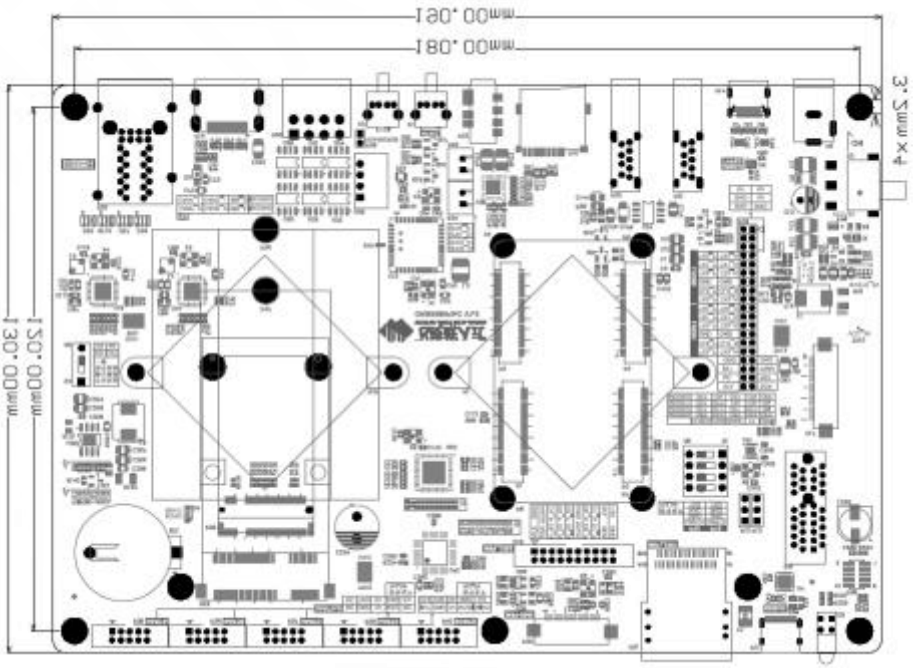
Chapter 3 OKMX8MPQ-C Carrier Board Features

3.1 Overview of OKMX8MPQ-C

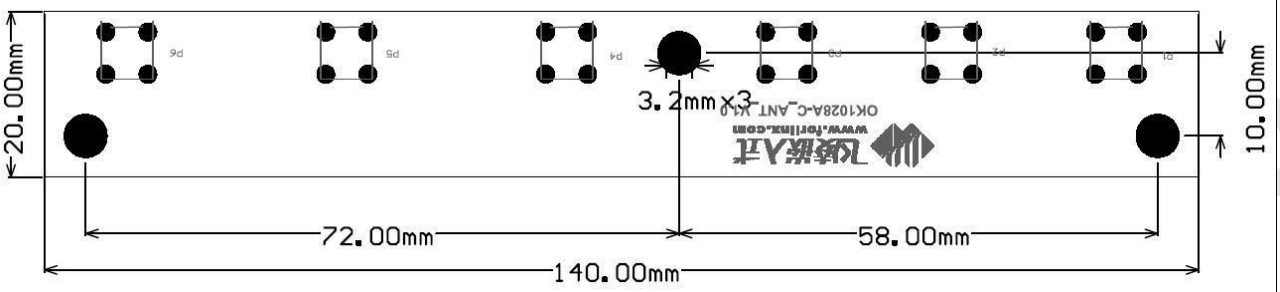
OKMX8MPQ-C single board computer consists of carrier board and SoM, the SoM can connect with carrier board by three ultra thin connectors.



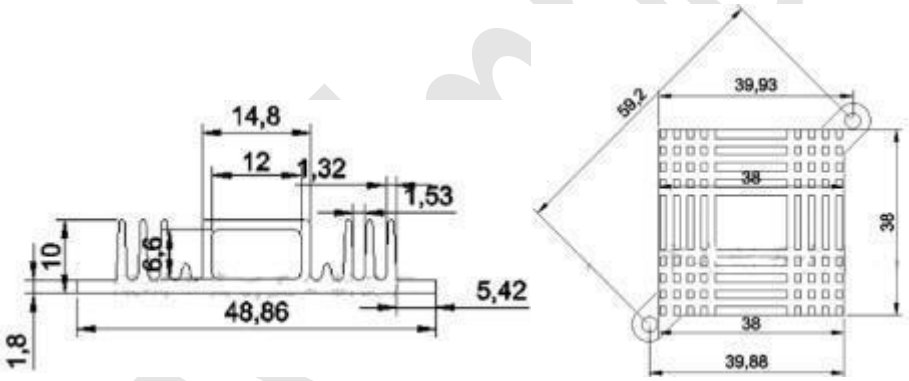
3.2 OKMX8MPQ –C Dimensions



PCB dimensions: 130mm x 190mm
Mounting hole: 120mm x 180mm, pore: 3.2mm
PCB: 4-layer, 1.6mm thickness
Power input: DC 12V
Antenna board is for installation of 4G/ 5G antennas, dimensions of 20mm* 140mm, more details please refer to below image



OKMX8MPQ-C carrier board is preserved with 2 mounting holes for heat sink with pore of 3.2mm, users can choose to equip the device with heart sink or not according the real condition, and please add a layer of insulated heat conduction silicone between heat sink and SoM.
Standard of the selected heat sink by Forlinx is 38mm* 38mm* 23mm, picture is as below



3.3 Carrier Board Features

Peripheral	QTY	Spec.
USB3.0 Type-C	1	USB3.0 Type-C, available for DFP, UFP and DRP
USB3.0	2	USB Type A header, only for Host
MIPI-CSI	2	CSI1: can support daA3840-30mc-IMX8MP-EVK, 3840* 2160 CSI2: 26-pin FPC connector and 2* 10-pin connector with pitch of 2.0mm, can support OV5645 module, up to 2592* 1944
MIPI-DSI	1	A 4-lane MIPI DSI by FPC connector on carrier board, can fit Forlinx 7'' MIPI DSI module very well, resolution 1024* 600@30FPS
LVDS	1	Dual async lanes(8 data, 2 clock), 1920* 1200p60
HDMI	1	HDMI2.0a, up to 4K@30FPS; HDMI2.1 eARC
Ethernet	2	10/ 100/ 1000Mbps auto-negotiation, RJ45 connector, one of them can support TSN
PCIe	1	PCieX1 connector on carrier board, PCI Express Gen3

TF card	1	Can support UHS-I TF card, up to 104MB/ s
4G/ 5G	1	Optional and alternative 4G: mini PCIe 4G wireless module, default driver: Quectel EC20 module; 5G: M.2 Key B 5G wireless module, default driver: Quectel RM500Q SIM card: Micro SIM card slot
WiFi	1	AW-CM358M; IEEE 802.11 a/b/g/n/ac dual-band WIFI, rate up to 433.3Mbps;
BT	1	Bluetooth 5, rate up to 3Mbps
Audio	1	On-board WM8960 chip Can support earphone output and MIC input, 1* 3.5mm jack; Can support 2* 1W8 Ω speaker output, by XH2.54 white header
IIC	3	For carrier board audio device, RTC, camera and other related devices mounting
PWM	2	for display backlight
RTC	4	4 on-board UART converted by USB, 2* 5-pin header with pitch of 2.0mm
UART	1	UART3: 3-wire, 3.3V, up to 4.0Mbps
ECSPI	1	2* 5-pin header with pitch of 2.0mm
CAN	2	Electrical isolation, can support CAN-FD, complies with CAN2.0B also
RS485	1	Electrical isolation, auto control transceiving direction
KEY	4	Power on/ off, reset keys, and extra 2 for users' definition
LED	2	for users' definition, red and green
DEBUG UART	2	3* 5-pin header with pitch of 2.0mm, integrated to USB Type-C for Cortex-A53 and M7 debug ports, default baud rate 115200
JTAG	1	2* 5-pin header with pitch of 1.27mm

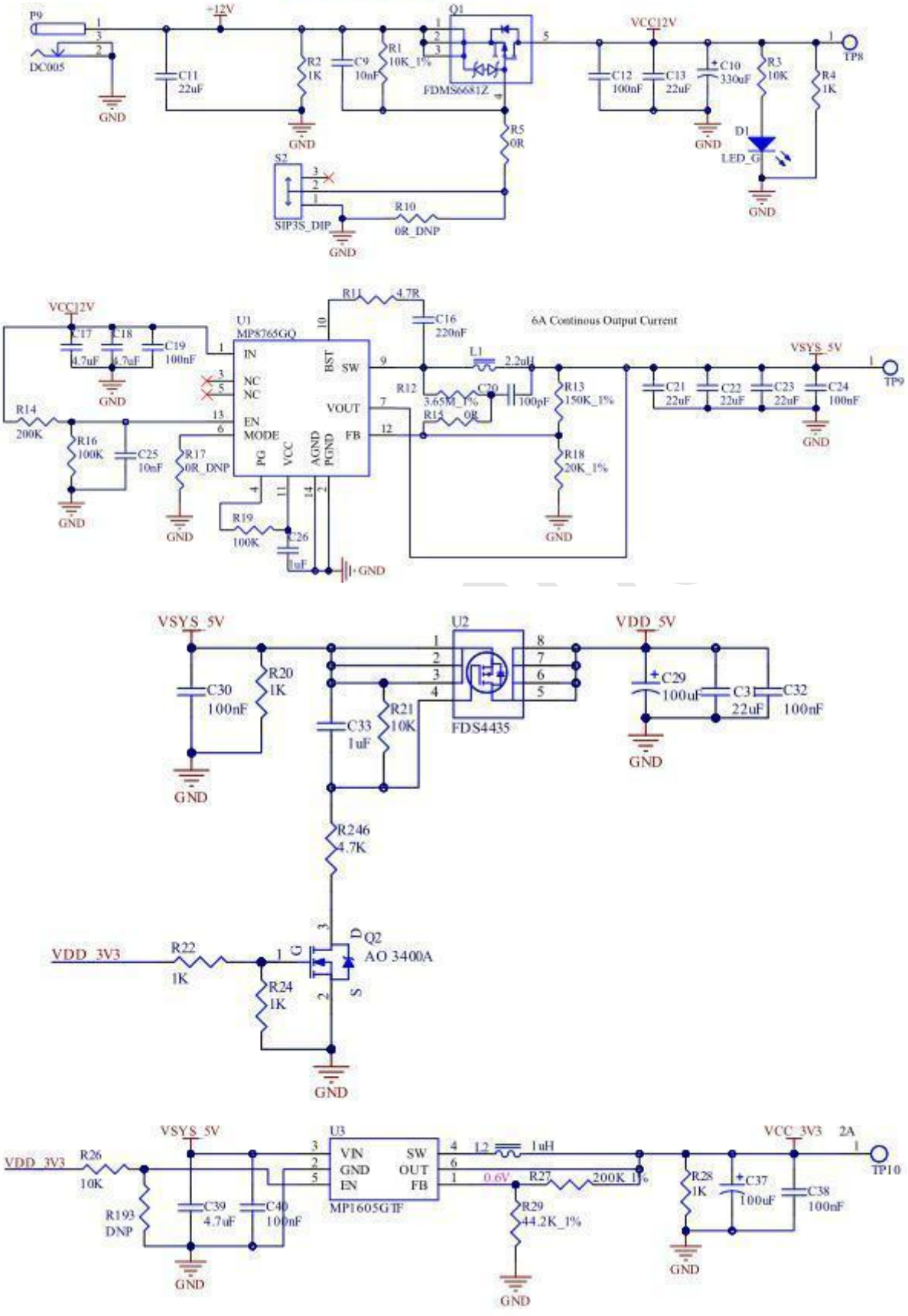
3.4 OKMX8MPQ-C Carrier Board Introduction

Note: components with marks of '_DNP' means the components are not soldered

3.4.1 Carrier Board Power

The 12V power adapter will supply power to development board by P9. VSYS_5V supplies power to SoM, once SoM is powered, it outputs VDD_3V3 to control carrier board U2 and u3 to be enabled.
VDD_3V3 makes the SoM powered firstly and then carrier board powered.
If users want to remove S2 power key in consideration of structure, please solder it with R10 resistor, so that the firmware could be powered automatically.
Note:
When users make carrier board designing, please refer to Forlinx carrier board power sequence that SoM outputs VDD_3V3 to enable carrier board DC-DC power, so that SoM can be powered firstly and then carrier board powered.

System Power



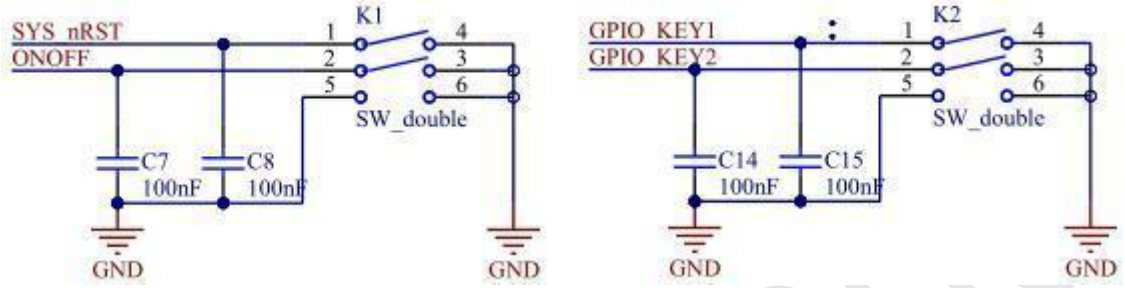
3.4.2 Key

SYS_nRST is a reset key.

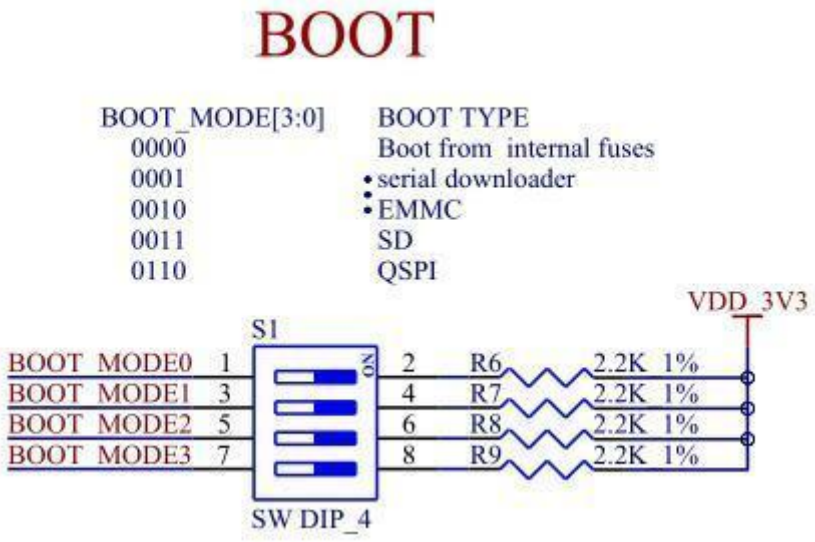
ONOFF is a power key, press it in ON mode, it will trigger a interrupt, and long press this key to power off it forced. Press this key in OFF mode, the internal power management status will switch to ON mode.

2x GPIO preserved for users' definition.

Note: SYS_nRST and ONOFF should be suspended when they are not needed, but please don't pull-up or pull-down.



3.4.3 Boot



There are 4 DIP switches S1 for booting mode selection.

Boot mode / DIP	Internal	Serial	EMMC	SD	QSPI
MODE3	OFF	OFF	OFF	OFF	OFF
MODE2	OFF	OFF	OFF	OFF	ON
MODE1	OFF	OFF	ON	ON	ON
MODE0	OFF	ON	OFF	ON	OFF

Internal fuses is used for booting medium selection by chipset internal fuse, which is not available by default, and it's not suggested to be used.

Serial downloader is generally used of firmware download by OTG, the development board takes P14 USB TypeC convert cable to be connected to PC, and then install firmware for the board.

eMMC: system boots from eMMC by default.

SD: the development board takes TF card for system guiding, thus to install firmware for the board by TF card

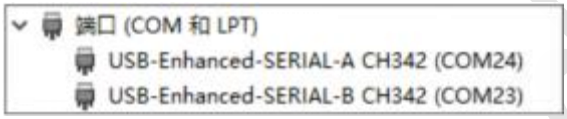
QSPI: system firmware boot from QSPI NorFlash.

Note:

The pulled-up voltage of BOOT signal is from VDD_3VS output from SoM.

3.4.4 Debug

There are 2 debug ports from SoM, UART2 is for A53 debug and UART4 is for M7 debug. It's drawn out to one USB port on carrier board by a USB to serial convert chip CH342F . To use debug port, please firstly install CH342F driver(http://www.wch.cn/products/CH342.html). Then take USB to Type C cable to connect development board P11 to USB port on PC, and in computer device management, it will generate 2 COM ports, A port is for A53 debug and B port is for M7 debug.

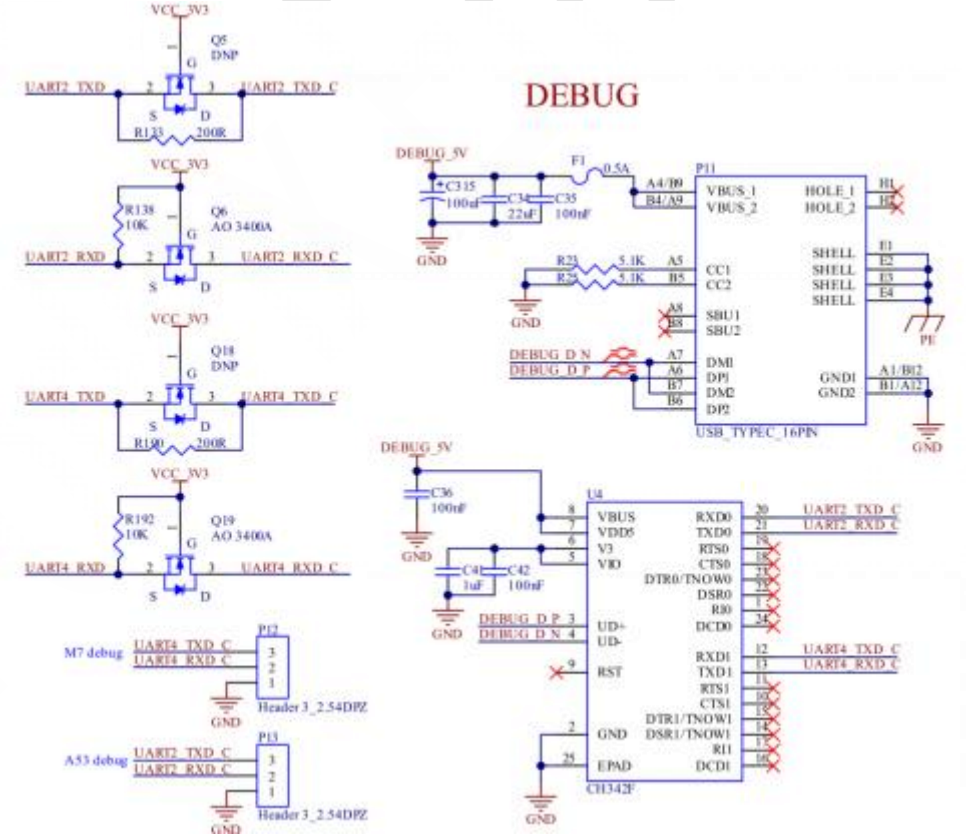


Open debug terminal tool on PC, such as Putty, and set baud rate to 115200, data bit 8, no parity bit, stop bit 1, choose correct COM port, and then power on development board to boot system, then we'll see serial output information.

Users can also take a UART convert cable to connect to P12 or P13.

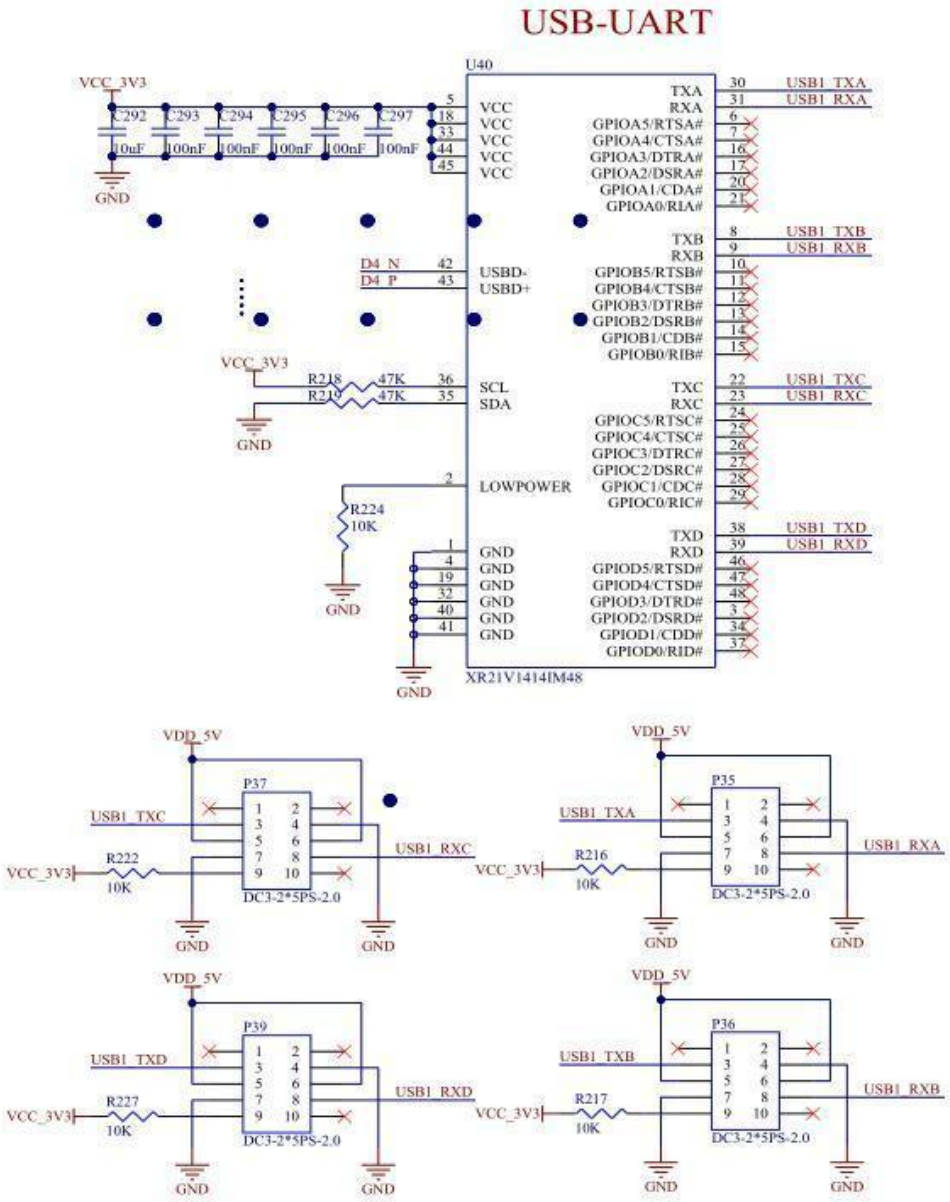
Note:

1. We kindly suggest users preserve debug port when designing PCB;
2. The debug port on carrier board designed with anti-creep solution for users' reference.



3.4.5 General UART

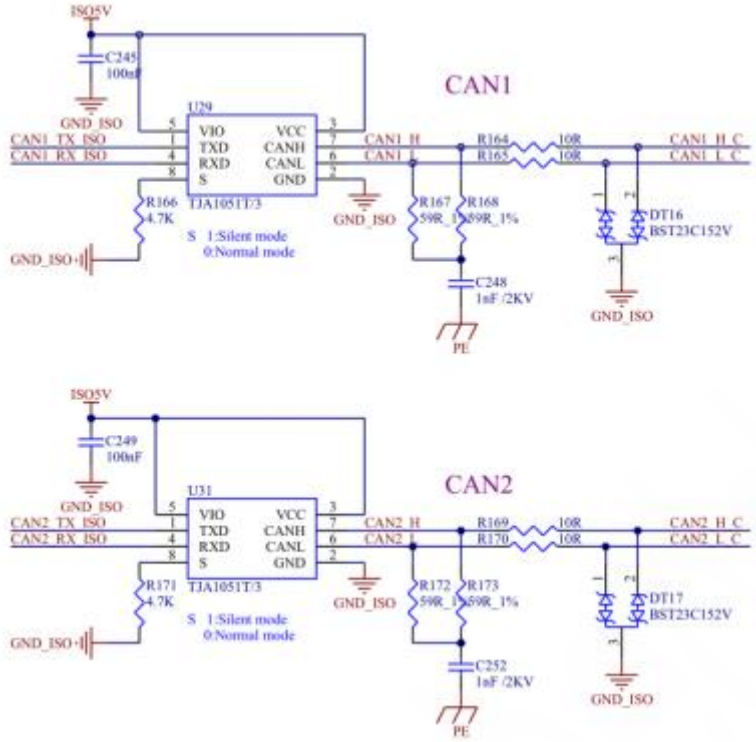
There are 4 general serial ports on carrier board, rate up to 12Mbps, designed as 2*5pin-2.0mm simple horn seat .



3.4.6 CAN

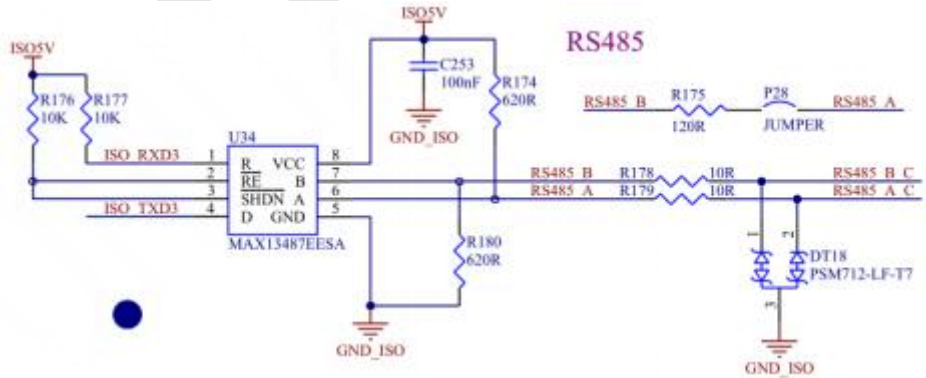
Two CAN ports are available on carrier board, comply with CAN-FD, designed with 1500VDC electrical isolation and ESD4 solution.

The headers are from P29, and we kindly suggest users to take it common-grounded when using it for communication.



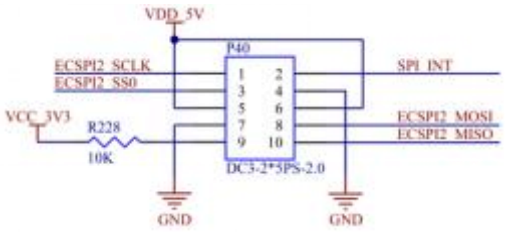
3.4.7 RS485

One RS485 from P29 is available on carrier board, designed with 1500VDC electrical isolation and ESD4 solution. MAX13487 can control transceiving direction automatically. P28 is short circuit jumper for 120 Ω resistor of AB wire. and we kindly suggest users to take it common-grounded when using it for communication.



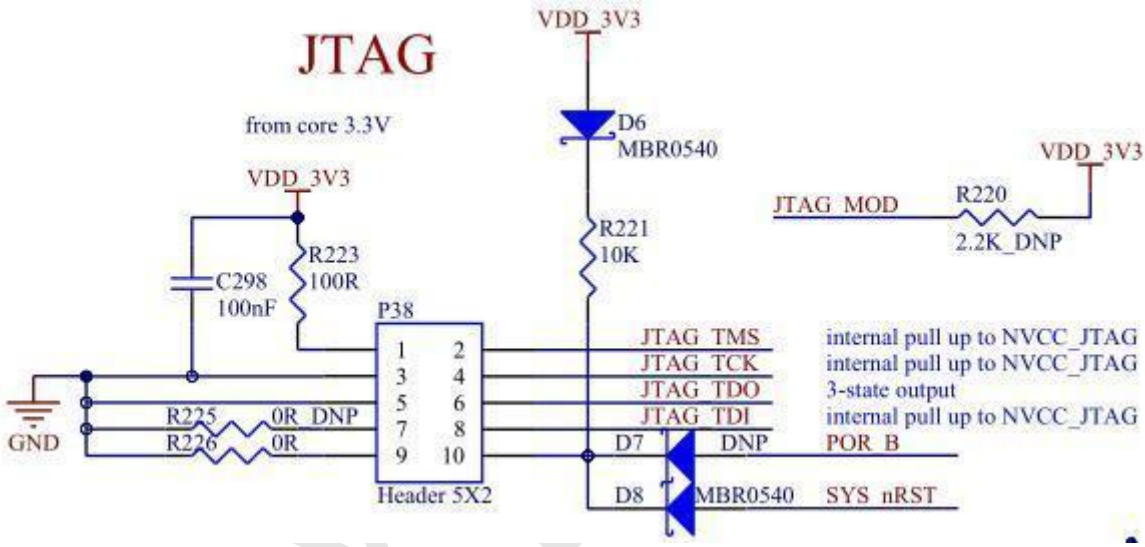
3.4.8 SPI

P40 on carrier board is a simple horn seat from ECSPI2.



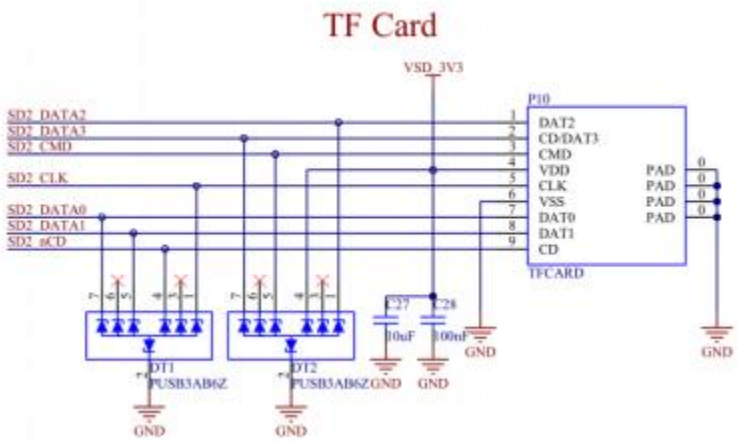
3.4.9 JTAG

P38 on carrier board with pitch of 1.27mm is a JTAG port, it could be suspended if not it's not needed.
BOOT_MODE[0:3], JTAG_MOD and POR_B should be up pulled to 111111 to get into i.MX8M Plus Boundary Scan mode



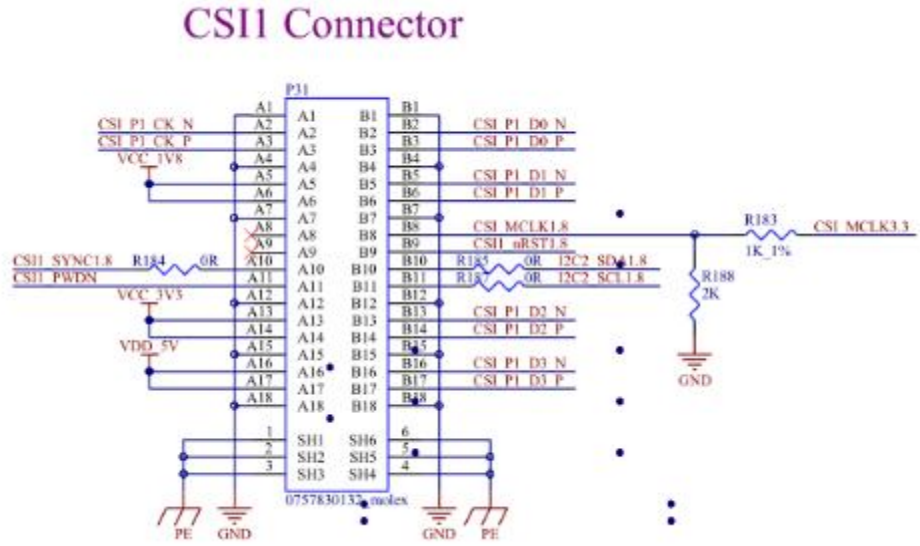
3.5.10 TF card

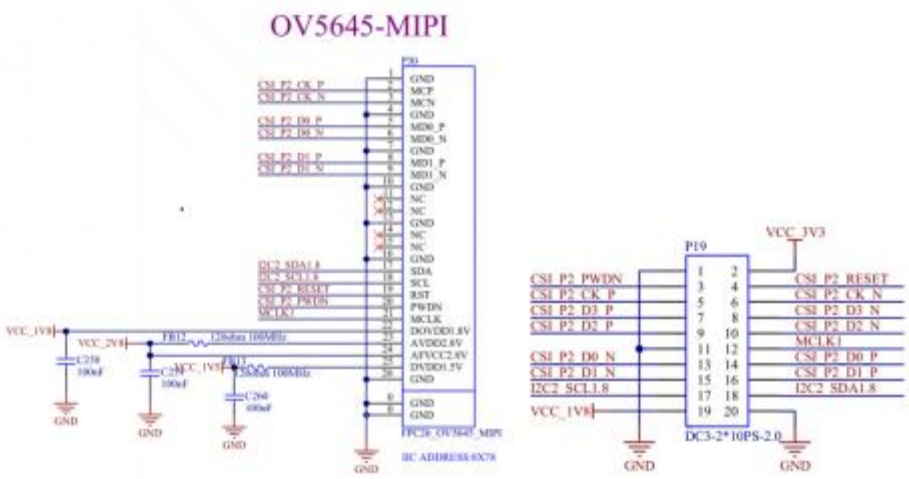
SD2 of CPU is for TF card, can support HS-I TF card, rate up to 104MB/s. TF card power supply VSD_3V3 is from the SoM, power supply current is 400mA.
Note:
1. bus pull-up resistor already equipped on SoM, please do not pull it up for carrier board.
2. TF card is a hot plug device, please design with ESD solution;
3. SD signal should be equal length processed



3.4.11 MIPI-CSI

The SoM has two MIPI-CSI interfaces, CSI 1 by P31 for daA3840-30mc-IMX8MP-EVK module, and CSI2 by a FPC(P30) connector for 2 lane MIPI-CSI, can be mounted with OV5645 camera module up to 2592x1944@15fps. All CSI2 signals are available for P19 which is convenient for users to debug other camera modules.



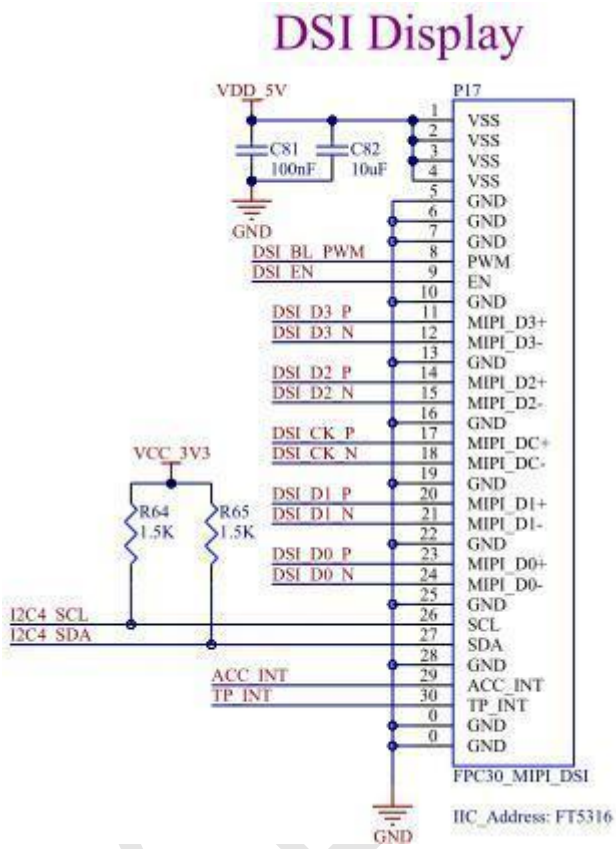


Note :

1. if users want to use other camera modules when designing PCB, there should be voltage transfer for IO;
2. MIPI should be with data equals with clock, differential impedance 100 Ω

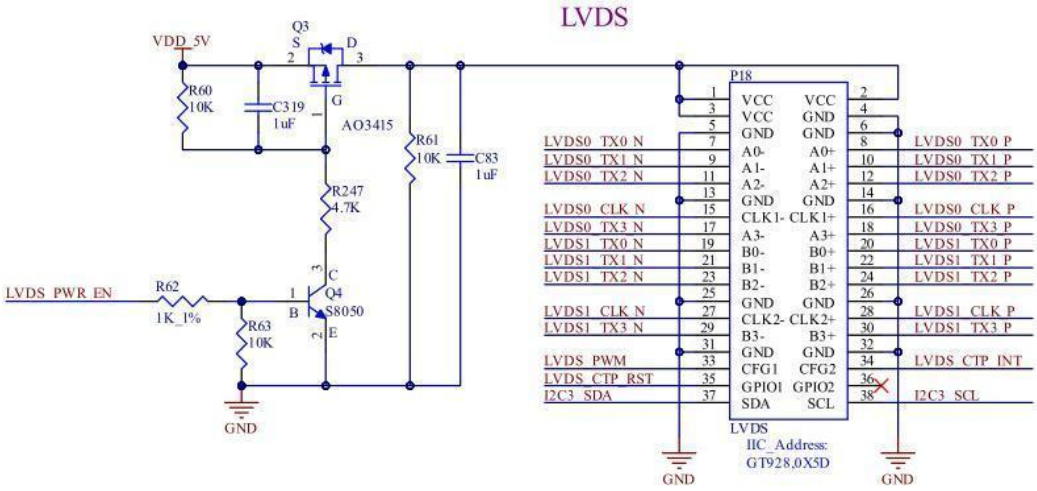
3.4.12 MIPI-DSI

The OKMX8MM-C is designed with a 4-lane MIPI_DSI as a 30-pin FPC connector with pitch of 0.5mm, it can support a 7'' MIPI display module designed by Forlinx.
Note: data should be equal with clock, differential impedance 100 Ω



3.4.13 LVDS

There are two 8-lane LVDS ports on carrier board by headers with pitch of 2.0mm, it can fit Forlinx 10.1'' LVDS module well, can support display brightness adjusting and capacitive touching.



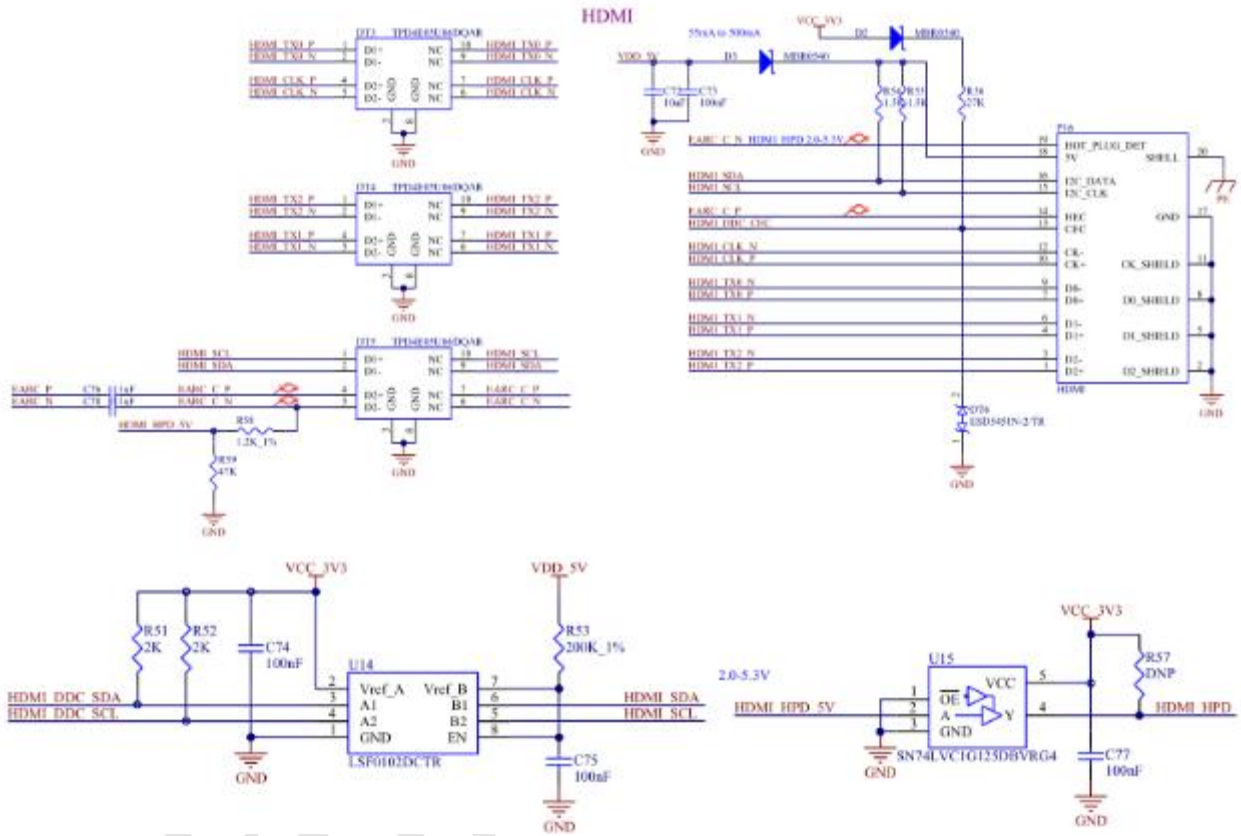
Note: data should be equal with clock, differential impedance 100 Ω

3.4.14 HDMI

One HDMI from P16 is available on carrier board, can support HDMI2.0a up to 4Kp30 and HDMI2.1 eARC, HDMI circuit contains level transfer circuit, users can take Forlinx circuit for reference

Note :

1. data should be equal with clock, differential impedance 100 Ω
2. HDMI is a hot plug port, please design it with ESD solution, and the chosen material should support HDMI2.0;
3. As 4K resolution is high quality requirement, please use specified cable to connect with the display.



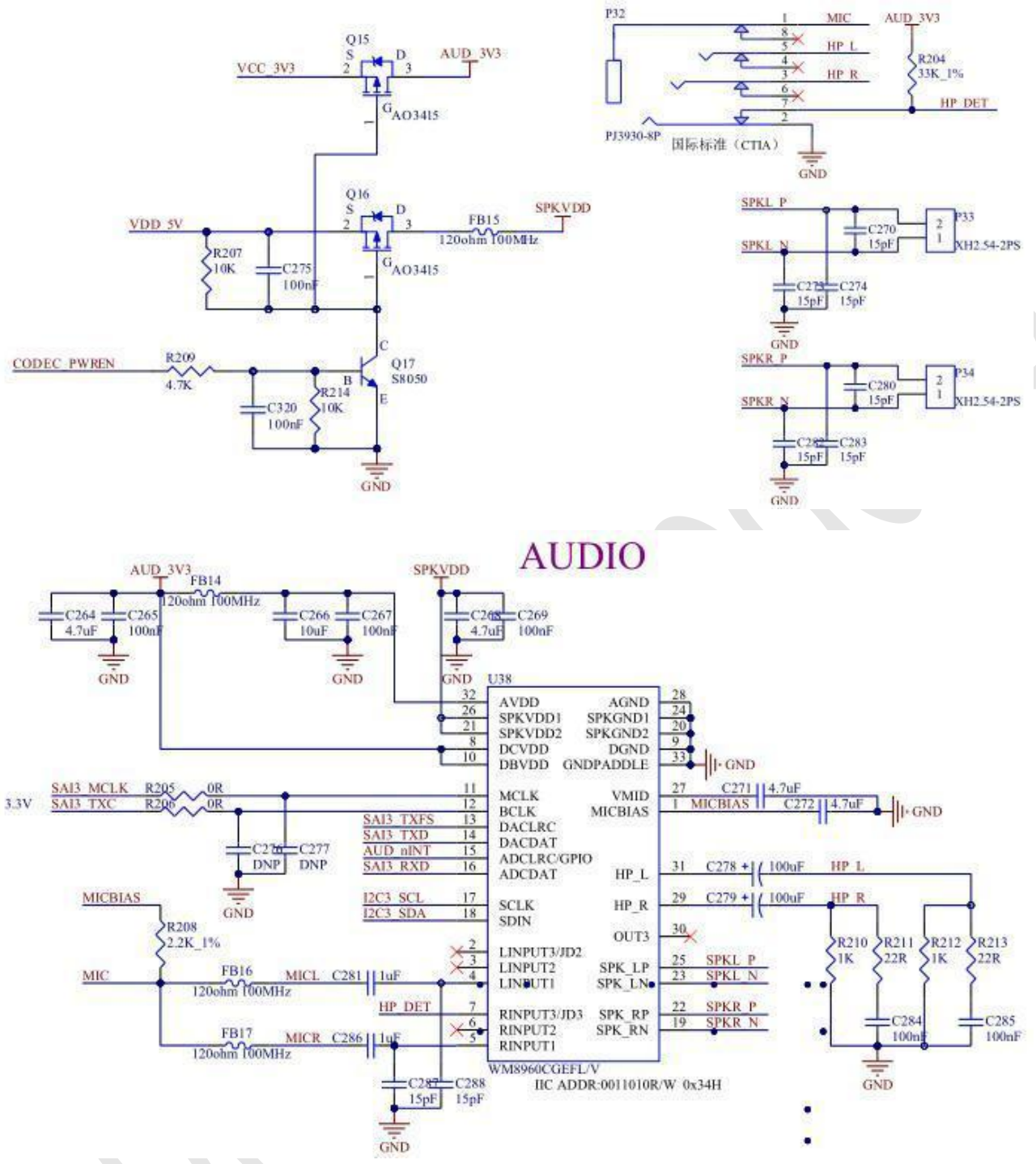
3.4.15 Audio

OKMX8MPQ-C is designed with audio WM8960 for SAI3 on carrier board can support two speaker output, supports dual track earphone output and one MIC input. It's designed as a 3.5mm jack on P32 with CTIA standard, if inserted with OMTP earphone, audio playback and record maybe get invalid. It can support earphone hot plug detection, when it's inserted with earphone, it will take output audio to earphone in priority.

WM8960 is built in with D amplifier up to 1W(8Ω),earphone driver consumption is 40mW(16Ω). to connect device with larger amplifier, it can only obtain signal from earphone but can not from speaker.

Note:

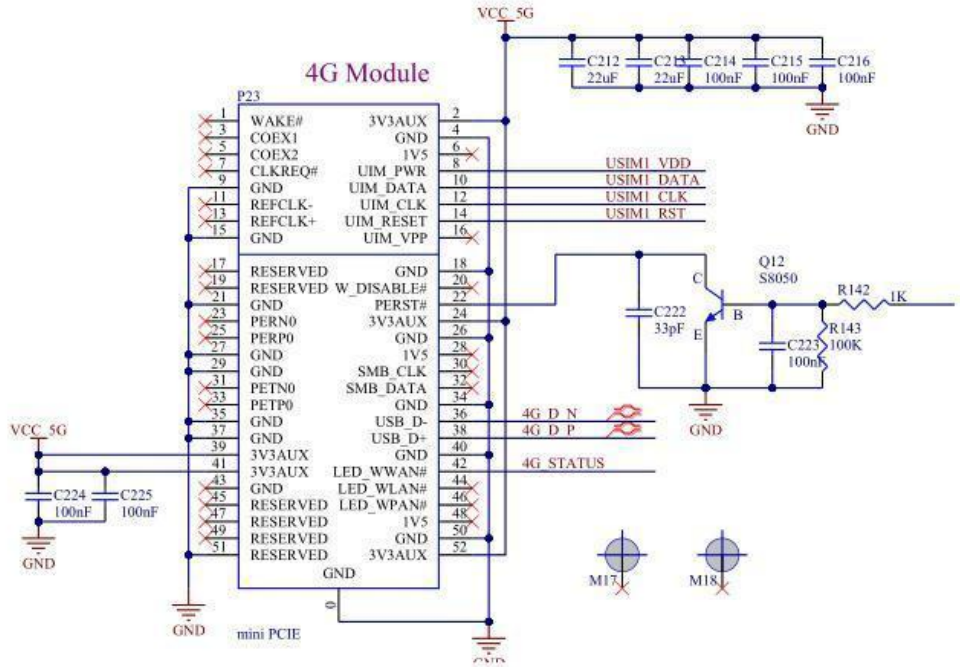
1. speaker's consumption is from D amplifier, but not typical analogy amplifier
2. please don't use speaker lines or circuit speaker to ground



3.4.16 4G/ 5G

4G and 5G are optional and alternative. Users can choose a mini PCIe standard 4G wireless module, the default one we use is Quectel EC20, and M.2 Key B standard 5G wireless module, the one we use is Quectel RM500Q.

4G and 5G share one DCDC power and one SIM card slot and also one USB2.0 channel, mount a module to board and set DIP to correct mode, then power on the board. When insert MicroSIM card, please don't reverse the direction.

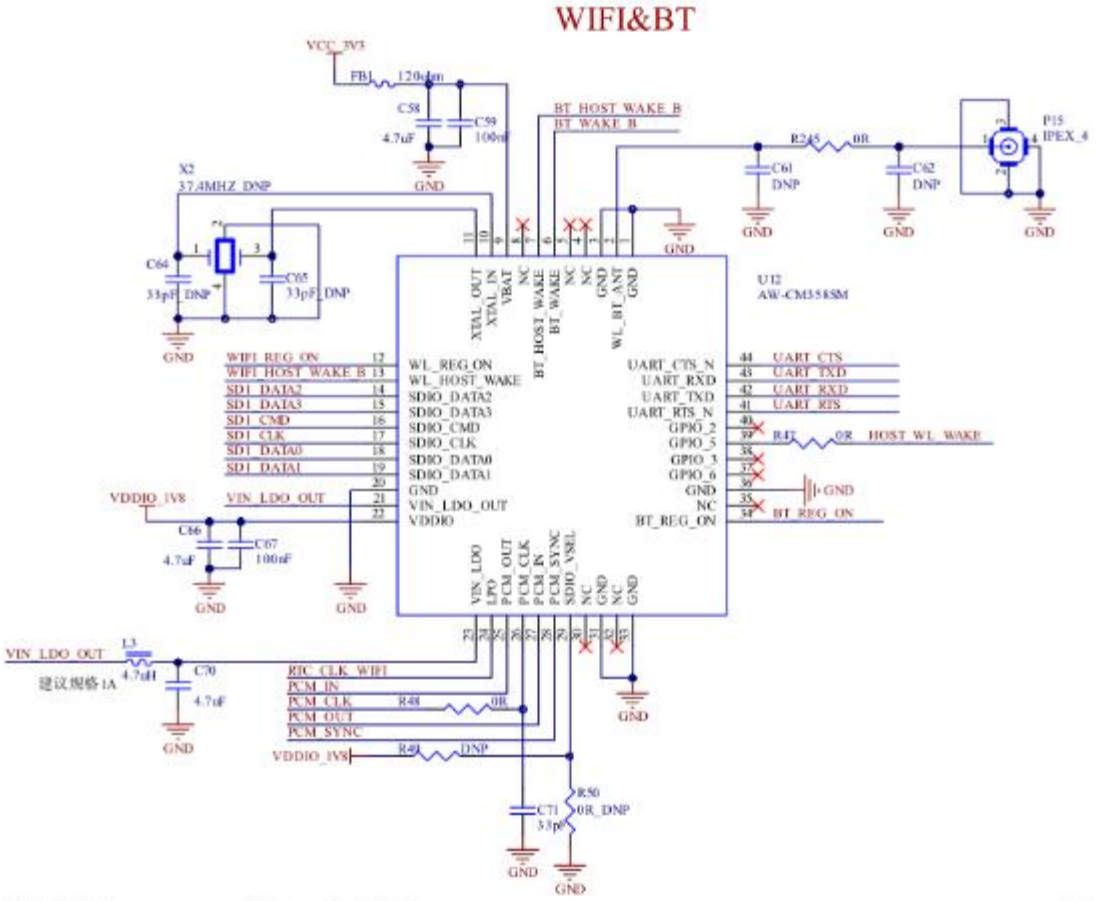


3.4.17 WIFI& BT

OKMX8MPQ-C is designed with an optional WIFI& BT module AW-CM358SM on carrier board, WLAN：IEEE 802.11 a/b/g/n/ac dual band WiFi up to 433.3Mbps, BT5.0 up to 3Mbps. Please use a 2.4& 5Ghz duan band antenna to enhance signal.

Note:

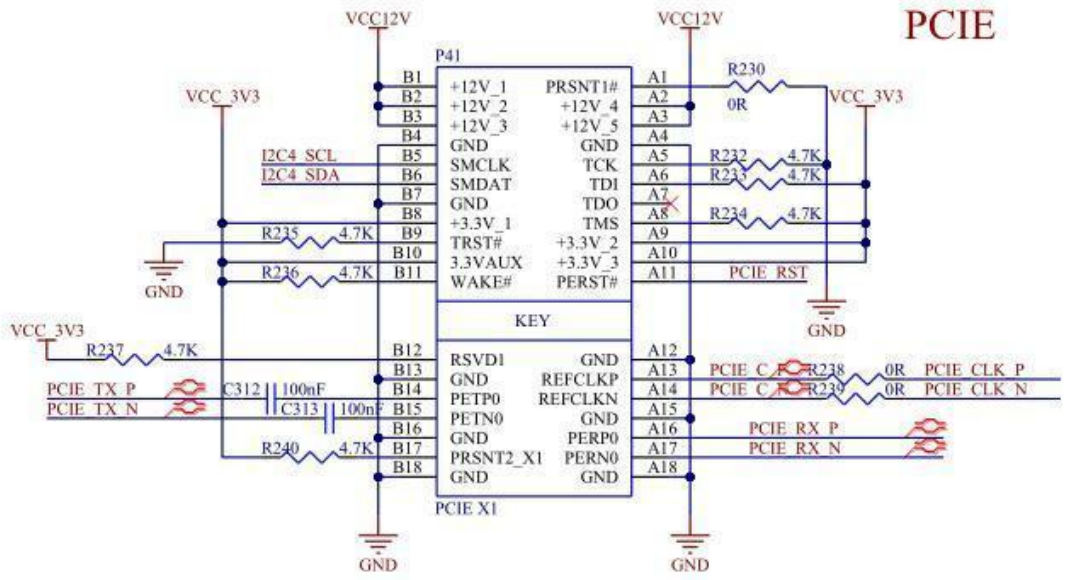
1. The module IO should be equipped with level transfer;
2. SD card signal should be processed with equal length.

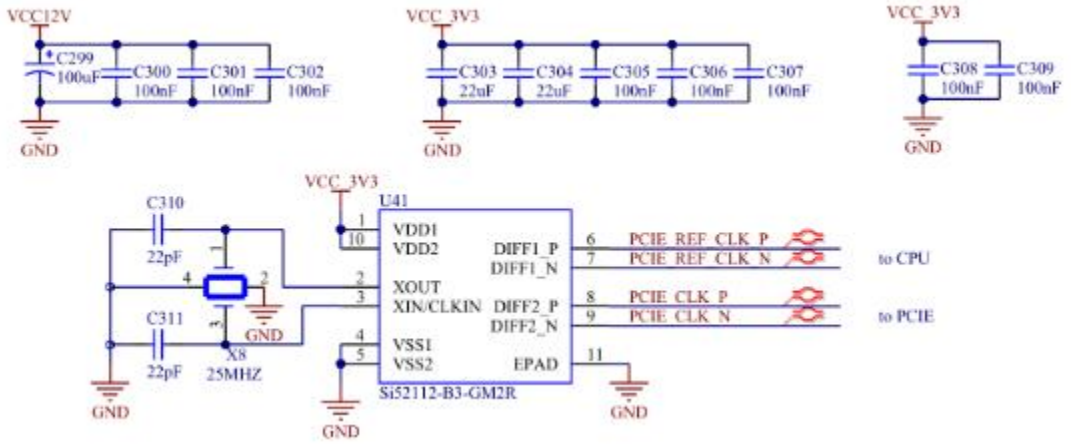


3.4.18 PCIe

One PCIe x1 slot with latch is available on OKMX8MPQ-C carrier board complies with PCI Express Gen3, PCIE_REF_CLK_P/N of SoM can only support input clock, it needs carrier board clock chip U42 with RC and EP with same source dual direction .

Note: PCIe TX/RX data and CLK reference clock both should be processed with 85Ω differential impedance.



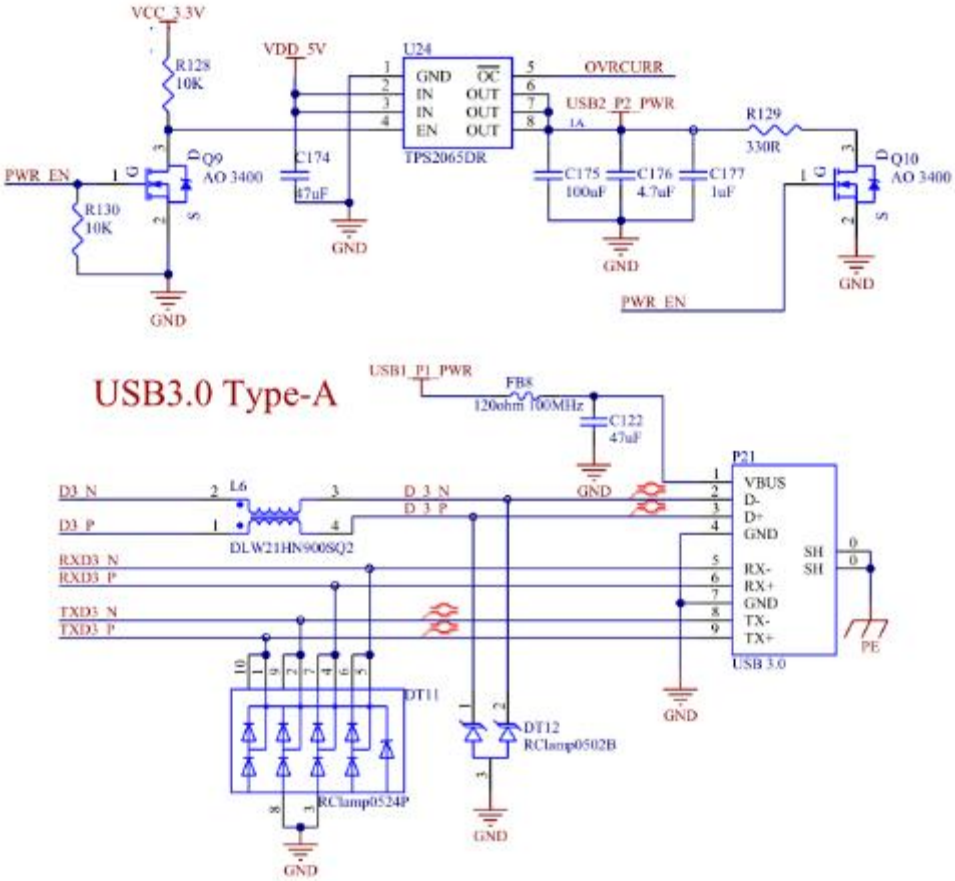


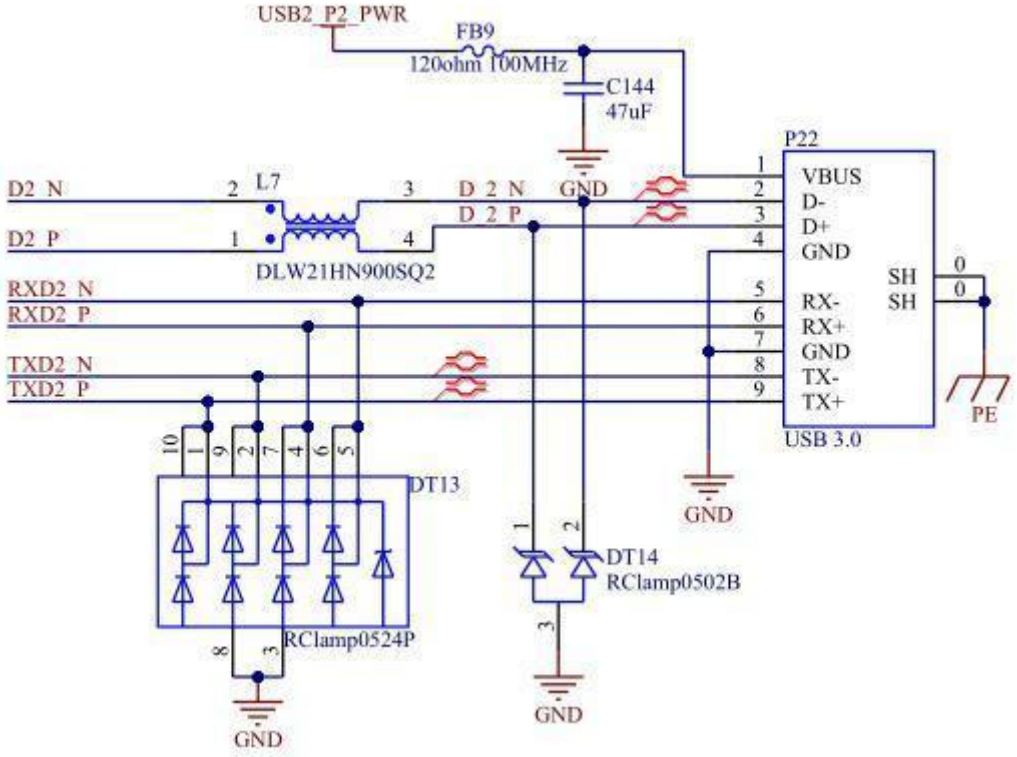
3.4.19 USB Host

It expand four USB3.0 to carrier board by USB3.0 HUB CYUSB3304, two of them are USB Type-A connectors with power anti short circuit protection, 1A limited, over-current protection controlled by USB HUB, if users don't use a HUB chip, please design short circuit protection circuit to carrier board.

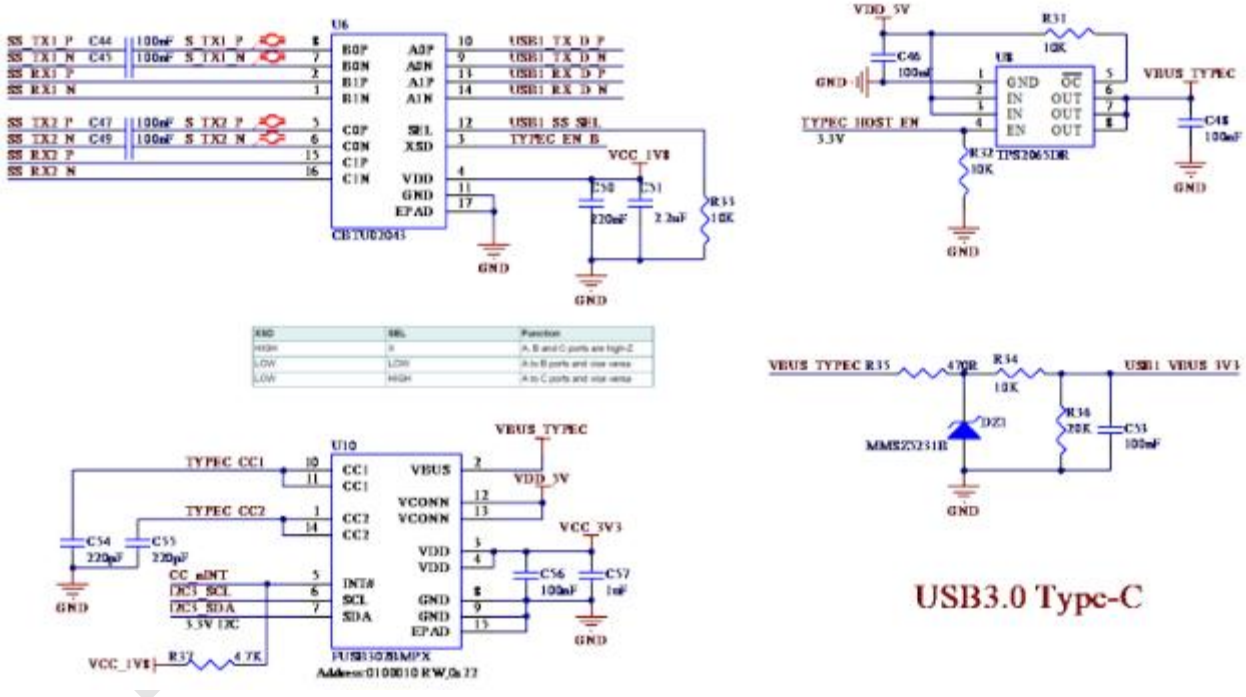
Note:

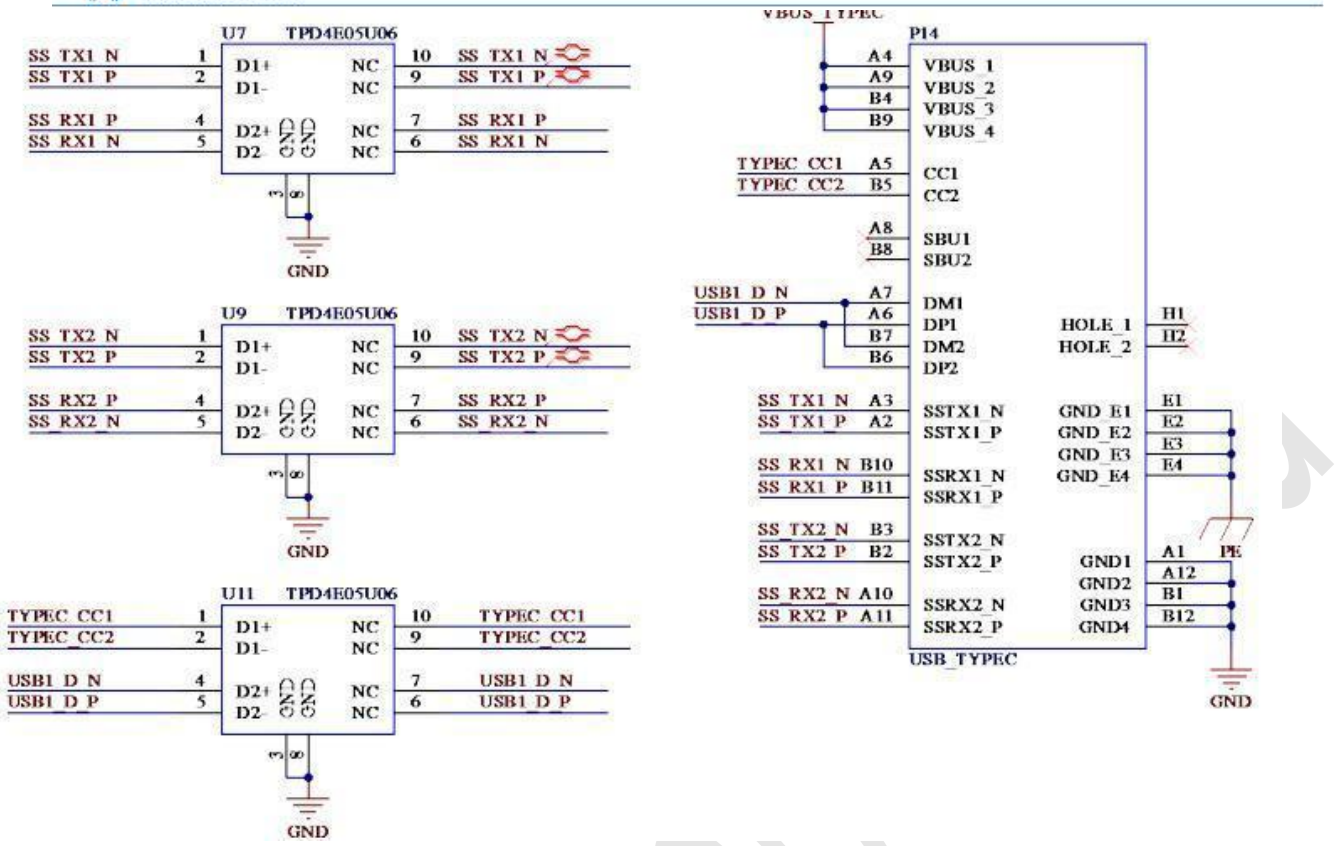
1. USB dta line should be processed with 90 Ω differential impedance;
2. Please choose a correct ESD component.



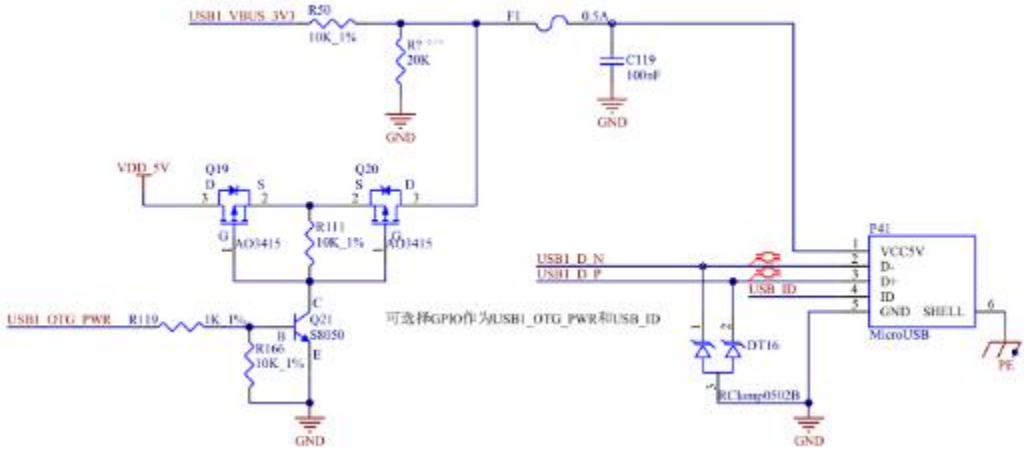


3.4.20 USB3.0 Type-C





There is one USB3.0 Type-C port on carrier board available for DFP, UFP and DRP for firmware installation. To get Type-C, the carrier board is designed with CC chip and USB Switch. Users can take Forlinx designing for reference. If users need USB2.0 OTG, the port can be simplified as below

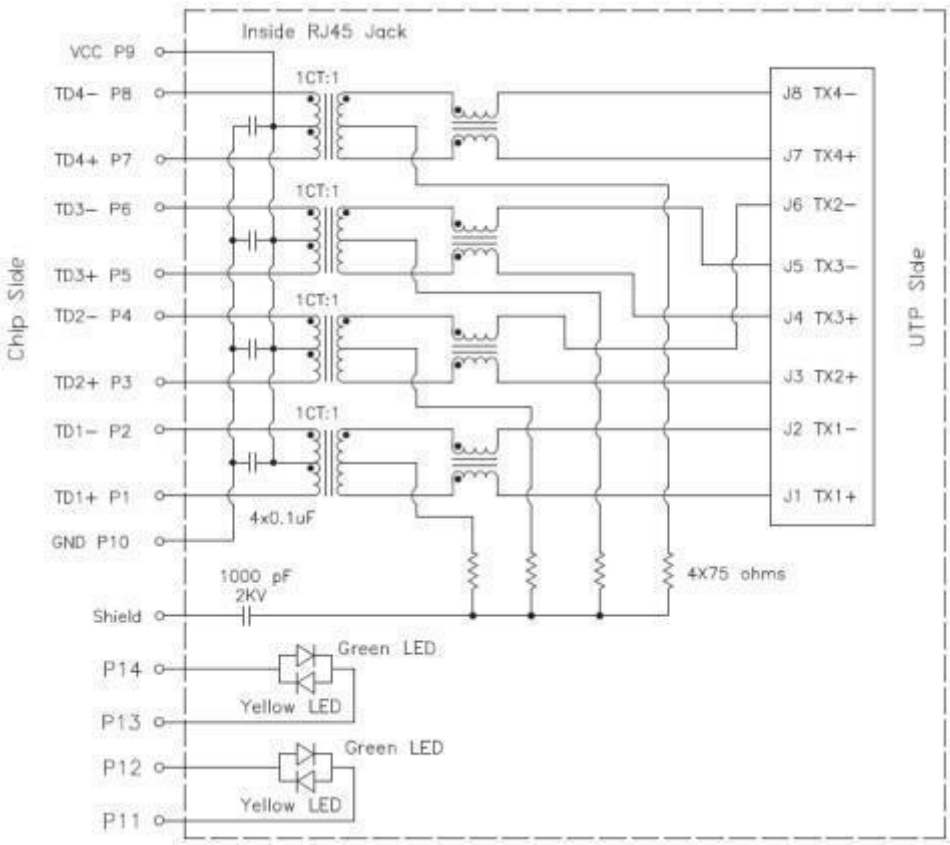


Note:

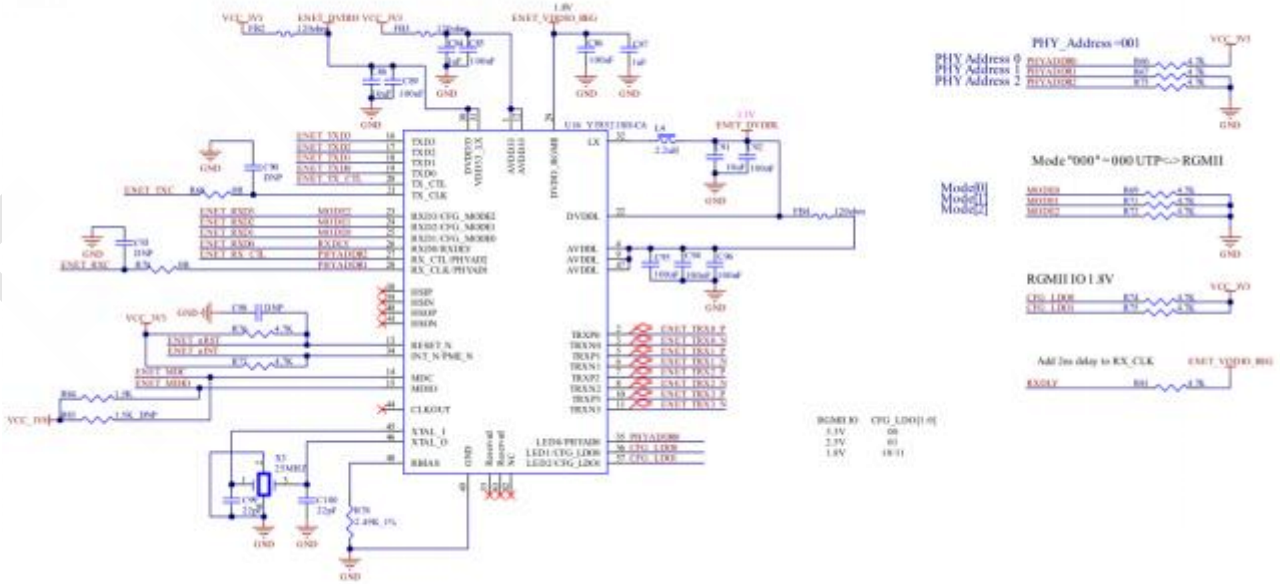
1. Only the SoM native USB1 can support USB OS image flashing;
2. USB data line should be processed with 90Ω differential impedance;
3. Please choose a correct ESD component;
4. USB function can be only enabled when USB1_VBUS_3V3 detects power voltage.

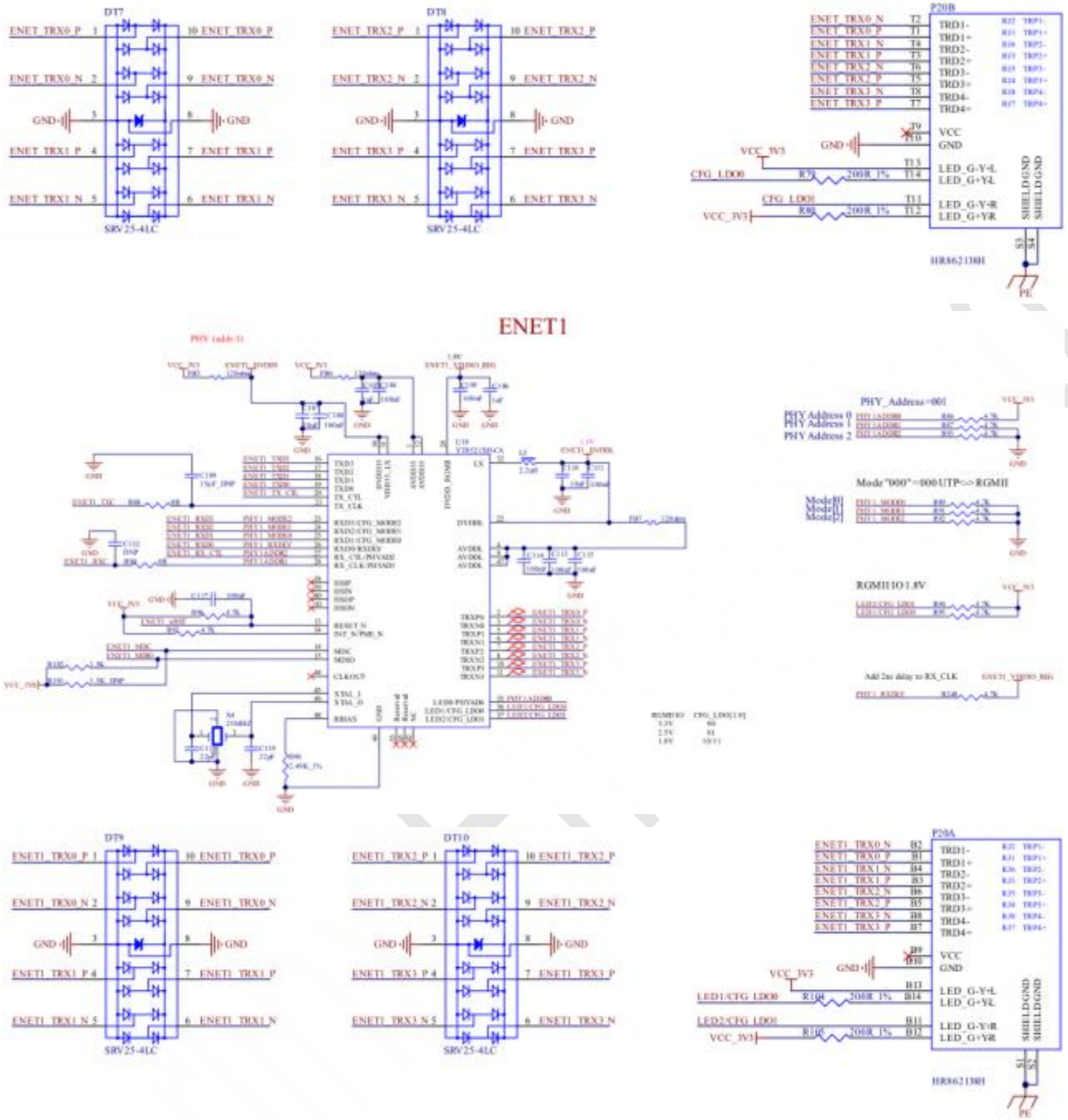
3.4.21 Ethernet

Two Gigabit Ethernet port (P20) are available on OKMX8MPQ-C carrier board and 10/100/1000Mbps auto-adaptive, the upper one can support TSN. SoM RGMII is mounted with PHY chip YT8521S , and the dual-layer RJ45 connector has internal network transformer and its structure is as below.



ENET_QoS with TSN



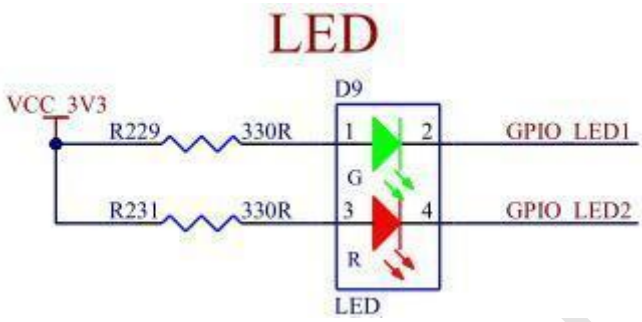


Note:

1. TX and RX of RGMII should be internal equal length.
2. RGMII and MDIO/ MDC should be compatible, it could be configured by CFG_LDO[1:0] ;
3. Please notice that unstable voltage may cause YT8521S failure;
4. Simulated differential line should be with 100Ω differential impedance, interclass equal length should be≤1000mil
5. The PCB should be designed with 4 layers at least and the circuit should be with complete reference layer, otherwise it may cause network failure;
6. It's kindly suggested to take Forlinx designing for reference.

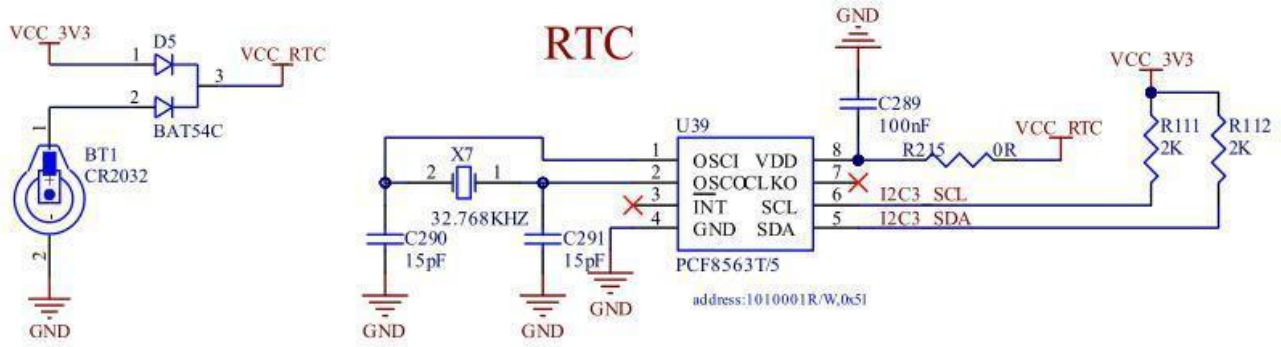
3.4.22 LED

2 LED indicators are available on carrier board controlled by GPIO and available for users' definition.



3.4.23 RTC

The carrier board mounted with RTC by IIC3 and be compatible with cell battery by VCC_3V3 from D5, when carrier board power is cut off, the battery can supply power to RTC chip. The circuit can be compatible with RS8010SJ and PCF8563T/5.



Appendix 1 Carrier Board Designing Tips

1. IIC

IIC can be mounted with multiple slave devices, please make sure addresses are not conflict;

IIC should be added with pull-up resistor, but please do not use multiple resistor pulled-up;

Please notice that SoM IIC voltage and slave device IIC voltage should be matched.

2. WDOG_B

On SoM, WDOG is circuited to power chip by GPIO of CPU, when CPU internal watchdog works, it will pull-down this signal to trigger power chip reset. It's suggested to be suspended on carrier board.

3. USB

USB_VBUS_3V3 is detection signal, its voltage should not exceed 3.6V, it can not directly circuited to VBUS_5V from USB connector.

To make MicroUSB to USB2.0 OTG, please take GPIO as ID pin for identity recognition;

To satisfy USB eye pattern demand, USB3.0 TX/RX PCB length should be less than 6 inches.

4. AD28_SD2_RESET_B

LD44 pin AD28_SD2_RESET_B is internal circuited to VSD_3V3 on SoM, used for reset carrier board SD card, please suspend it on carrier board.

5. R26_NAND_DQS

RU75 pin R26_NAND_DQS should be suspended.

6.Signals not used by SoM could be suspended, but please circuit all of them to GND.

7.power sequence

We kindly suggest users taking Forlinx carrier board designing for reference, take VDD_3V3 output from SoM to enable carrier board power, strictly control power sequence, otherwise, it may cause below problems

Power on current over large;

Device booting failure;

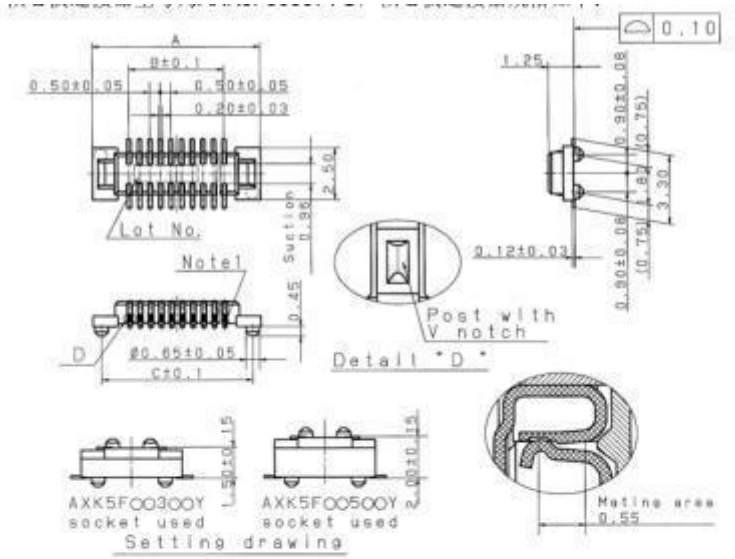
CPU failure

7. about IO power leakage

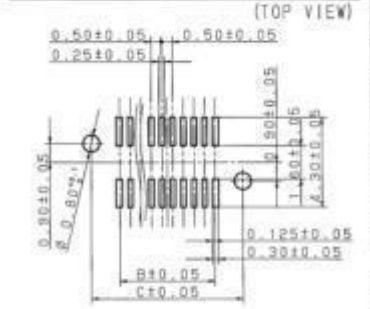
Before the SoM is powered on, if there are SoM pins with high level sink current, it will supply power to SoM, the red indicator on SoM will shine, and it will detect VDD_3V3 power, which may cause incorrect power sequence, thus to cause serial power leakage. So the debug port on carrier board is designed with anti-leakage circuit. Users can take Forlinx designing for reference.

Appendix 2 Connector

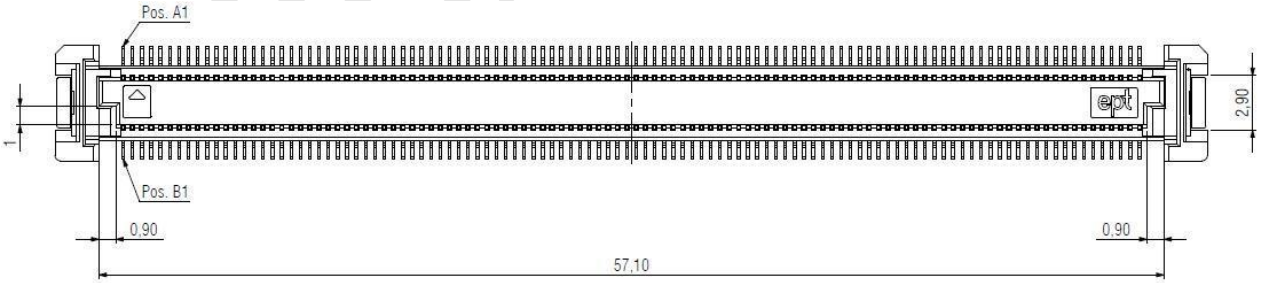
connector model on SoM is AXK6F80337YG



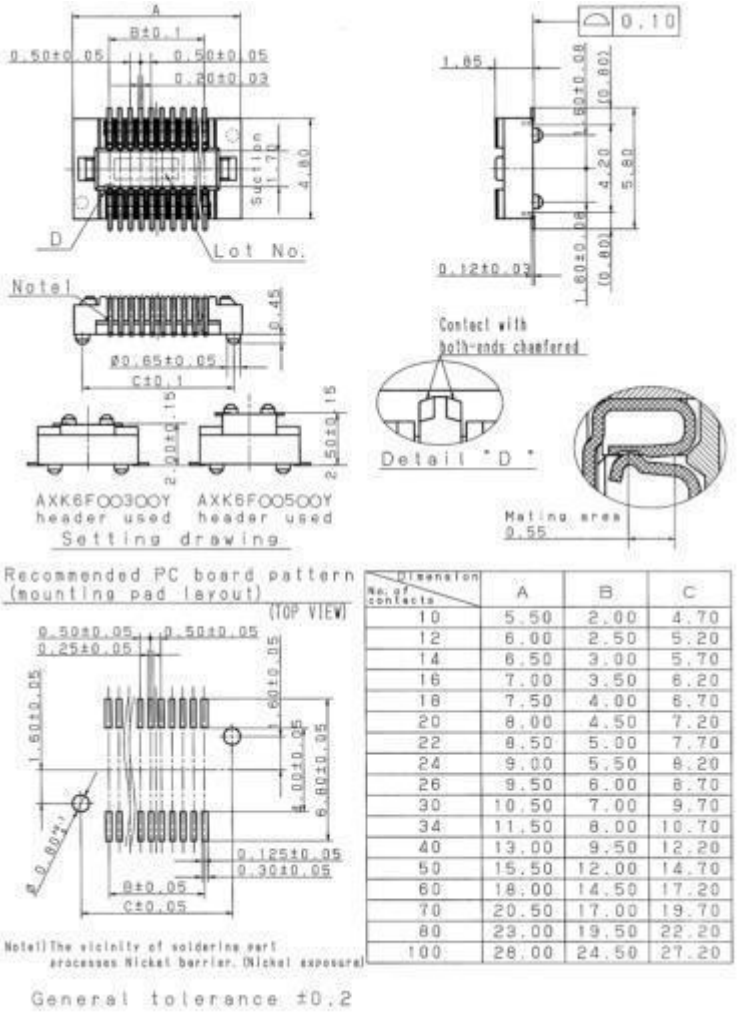
Recommended PC board pattern (mounting pad layout)



No. of contacts \ Dimension	A	B	C
10	5.50	2.00	4.70
12	6.00	2.50	5.20
14	6.50	3.00	5.70
16	7.00	3.50	6.20
18	7.50	4.00	6.70
20	8.00	4.50	7.20
22	8.50	5.00	7.70
24	9.00	5.50	8.20
26	9.50	6.00	8.70
30	10.50	7.00	9.70
32	11.00	7.50	10.20
34	11.50	8.00	10.70
40	13.00	9.50	12.20
50	15.50	12.00	14.70
60	18.00	14.50	17.20
70	20.50	17.00	19.70
80	23.00	19.50	22.20
100	28.00	24.50	27.20



The connector matched on carrier board is AXK5F80537YG



Dimension / No. of contacts	A	B	C
10	5.50	2.00	4.70
12	6.00	2.50	5.20
14	6.50	3.00	5.70
16	7.00	3.50	6.20
18	7.50	4.00	6.70
20	8.00	4.50	7.20
22	8.50	5.00	7.70
24	9.00	5.50	8.20
26	9.50	6.00	8.70
30	10.50	7.00	9.70
34	11.50	8.00	10.70
40	13.00	9.50	12.20
50	15.50	12.00	14.70
60	18.00	14.50	17.20
70	20.50	17.00	19.70
80	23.00	19.50	22.20
100	28.00	24.50	27.20

Appendix 3 Power Consumption Sheet

OS Linux

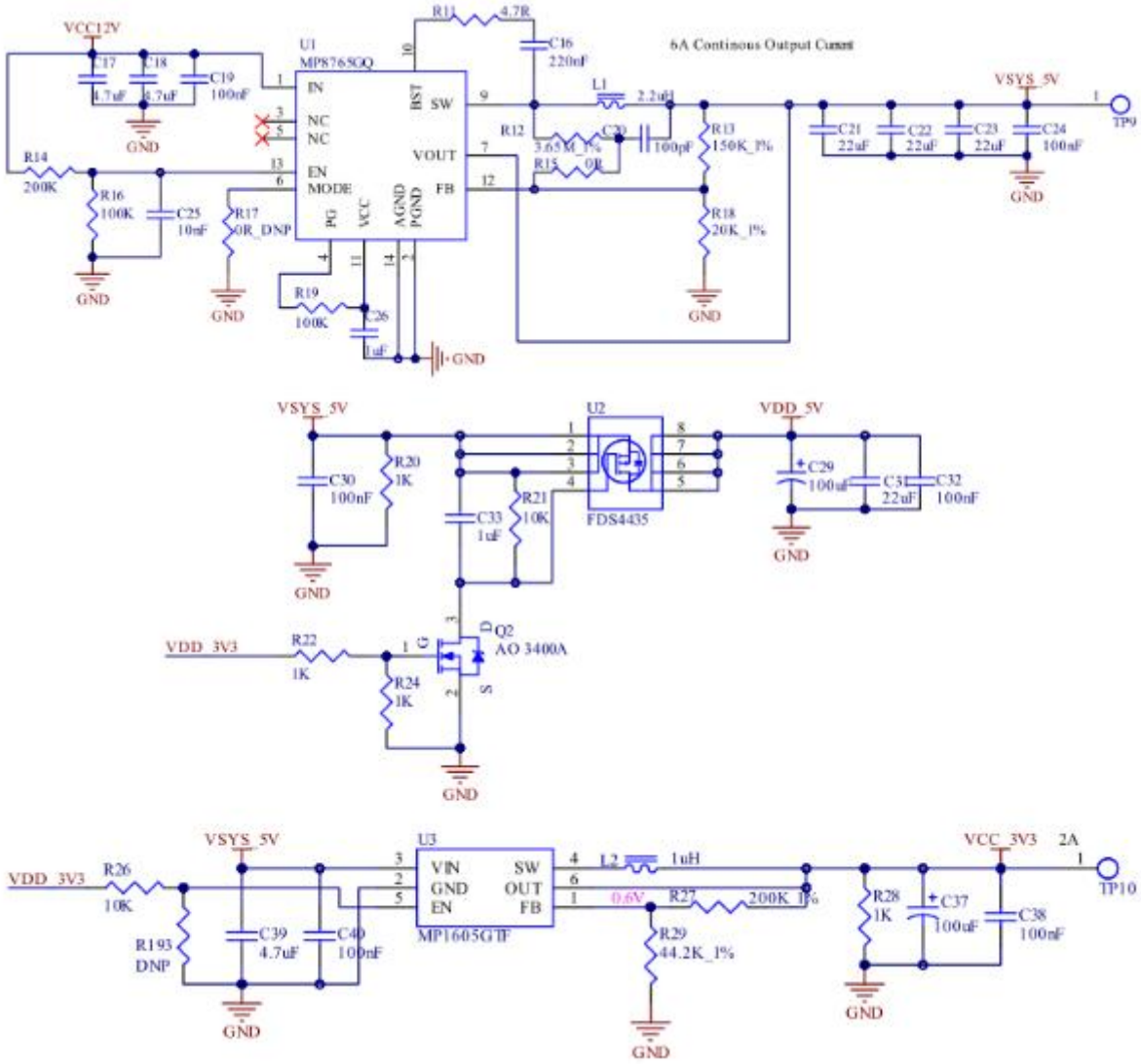
Hardware	Test	Voltage in (V)	Current output	
			Instant Peak(mA)	Stable(mA)
OKMX8MPQ-C	OKMX8MPQ-C mounted with PCIe hard disk, 5G, 10.1'' LVDS display with video playing	12	1.07	0.89
FETMX8MPQ-C	Powered with empty loaded	5	0.72	0.42
	CPU 100% loaded	5	-	0.57
	Sleeping mode	5	-	0.105

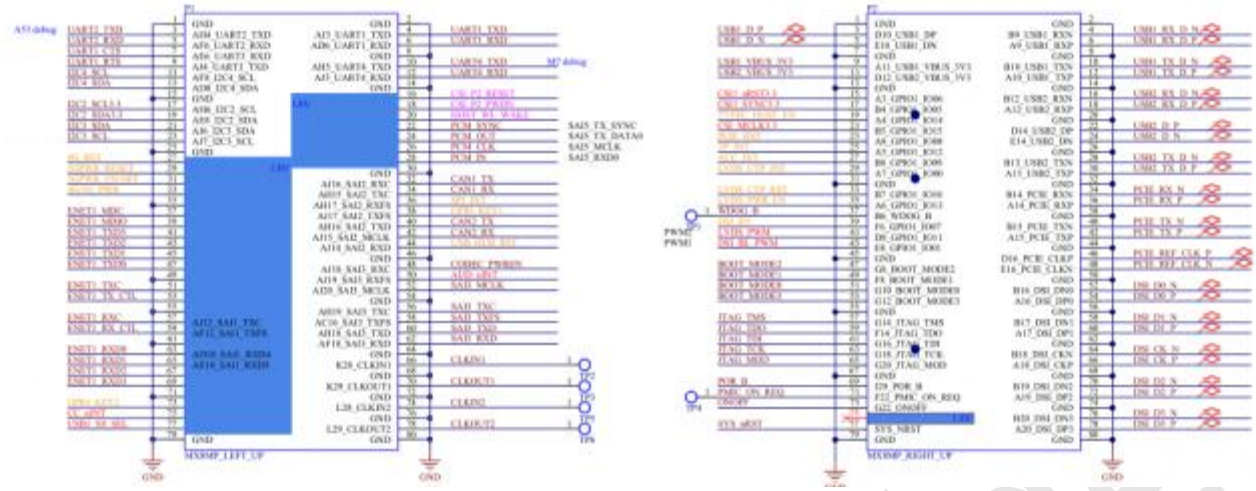
Note:

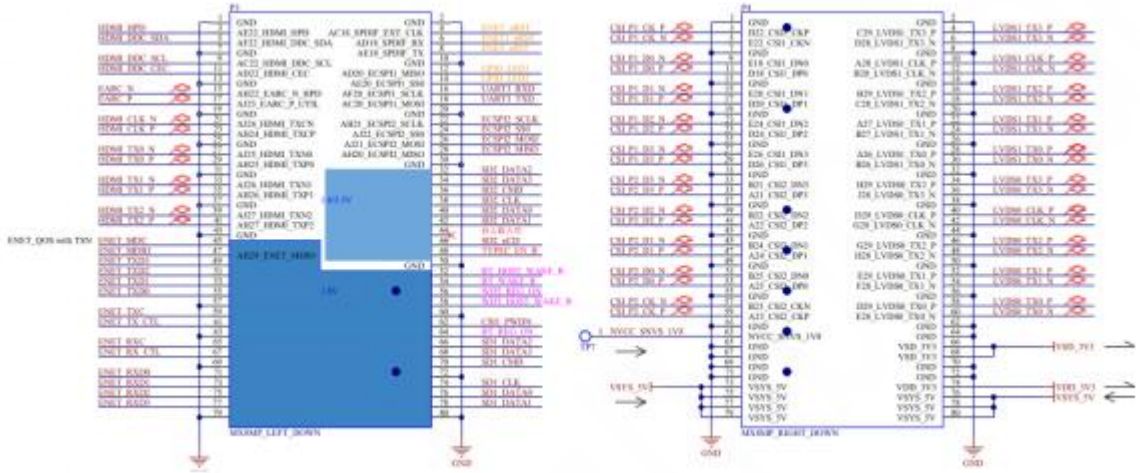
1. Peak current: the maximum current during system booting
2. Stable current: current of system booted and stay at splash interface.

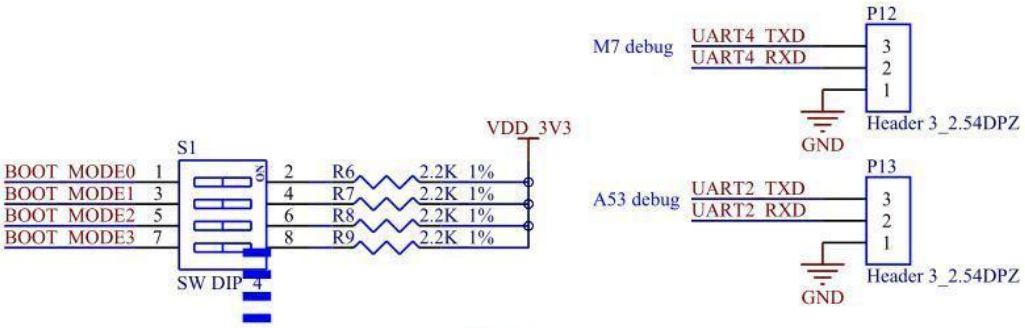
Appendix 4 Minimum System Schematic

Below pictures are just for reference. To make sure the SoM can work, except for VSYS_5V, it also needs SyS_nRST, BOOT configuring circuit, OTG or SD card, which will be convenient for users for firmware installation and system boot; UART2 and UART4 circuit will be convenient for users to do debug operation and check system status.

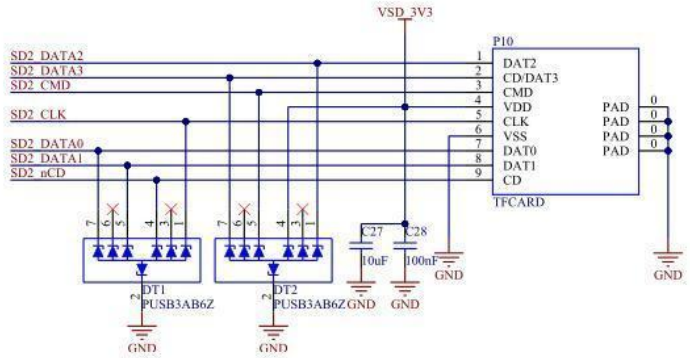







M7 debug
UART4_TXD
UART4_RXD
P12
3
2
1
GND
Header 3_2.54DPZ
A53 debug
UART2_TXD
UART2_RXD
P13
3
2
1
GND
Header 3_2.54DPZ
VDD_3V3
S1
BOOT_MODE0 1
BOOT_MODE1 3
BOOT_MODE2 5
BOOT_MODE3 7
ON
2
4
6
8
R6 2.2K 1%
R7 2.2K 1%
R8 2.2K 1%
R9 2.2K 1%
SW DIP-4

TF Card


VSD_3V3
P10
SD2_DATA2
SD2_DATA3
SD2_CMD
SD2_CLK
SD2_DATA0
SD2_DATA1
SD2_nCD
DAT2
CD/DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
CD
PAD
TFCARD
C27
10uF
C28
100nF
DT1
PUSB3AB6Z
DT2
PUSB3AB6Z
GND