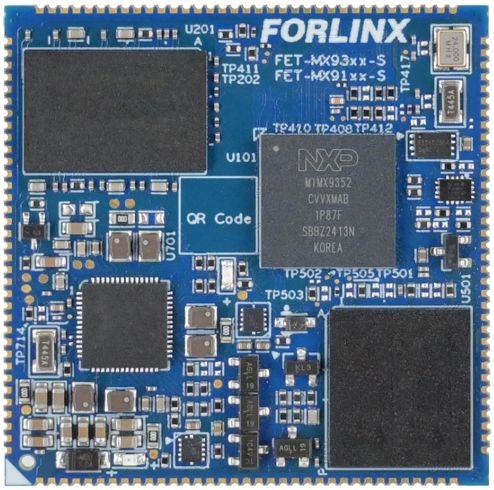
FET-MX9352-UP4 SoM

The FET - MX9352 - UP4 SoM is developed based on the NXP i.MX9352 processor. It features 2 x Cortex-A55 cores and 1 x Cortex-M33 real-time core, achieving a maximum main frequency of up to 1.7 GHz. It natively supports several common interfaces, including 8 x UART, 2 x Ethernet (with 1 x supporting TSN), 2 x USB 2.0, and 2 x CAN-FD. Additionally, the processor incorporates a Neural Processing Unit (NPU) that accelerates edge machine learning applications. Its compact size makes it easy to integrate into various products.

It has undergone thorough testing in industrial environments by Forlinx Embedded Laboratory to ensure stability and reliability. 10 to 15 years longevity, ensuring a consistent supply over time.



2×A55+1×M33	1.7 GHz	0.5 TOPS
Architecture	Clock	NPU
CAN-FD	TSN	UP4 package
2	Ethernet	Compatibility

Product Features:

- Multi - core heterogeneous architecture of A - core + M - core combines multi - task processing and real - time control;
- 0.5 TOPS Ethos U - 65 microNPU, meeting the requirements of edge AI;
- 2 x Gigabit Ethernet ports, 1 x supports TSN.
- LCC+LGA package (compact size);
- Universal package and is compatible with the UP4 series of SoMs.

SoM Parameter:

Processor	**NXP i.MX9352** **CPU：** 2×Cortex-A55@1.7GHz+1×Cortex-M33@250MHz **NPU：** 0.5 TOPS
RAM	1GB LPDDR4
ROM	8GB eMMC
Operating Voltage	DC 5V
Operating Temperature	-40℃ ~ +85℃
Connection	LCC + LGA (487 pins, pin center pitch of stamp hole is 1mm, single pin size: 0.7 * 0.6mm, ball pitch of LGA is 1.27 mm, single ball diameter is 0.8mm)

SoM Function Parameters:

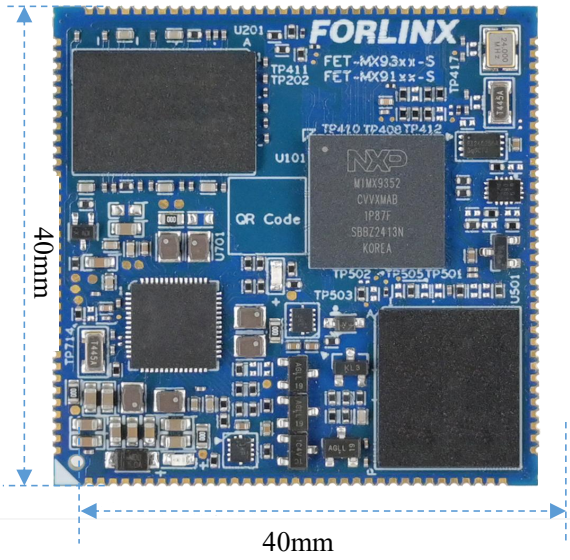
Function	Maximum Number	Parameter	UP4 defines the number of interface resources	Parameter
MIPI CSI	≤1	• Compatible with MIPI CSI - 2 v1.3 and MIPI D - PHY v1.2 specifications; • Supports up to 2 Rx data channels (plus 1 Rx clock channel); • The pixel clock can reach 200MHz, and the pixel fill rate can reach up to 150Mpixel/s under nominal voltage and over - speed voltage; • Data rate ranges from 80Mbps to 1.5 Gbps in high - speed mode and is 10Mbps in low - power mode.	**1**	• Compatible with MIPI CSI - 2 v1.3 and MIPI D - PHY v1.2 specifications; • Supports up to 2 Rx data channels (plus 1 Rx clock channel); • The pixel clock can reach 200MHz, and the pixel fill rate can reach up to 150Mpixel/s under nominal voltage and over - speed voltage; • Data rate ranges from 80Mbps to 1.5 Gbps in high - speed mode and is 10Mbps in low - power mode.
Ethernet	≤2	Supports 2 x RGMII interfaces and complies with IEEE 802.02 specification, 1 x supports TSN and 2 x support IEEE 1588 standard.	**2**	Supports 2 x RGMII interfaces and complies with IEEE 802.02 specification, 1 x supports TSN and 2 x support IEEE 1588 standard.
LCD	≤1	24-bit parallel RGB up to 1366x768p60 or 1280x800p60.	**1**	24-bit parallel RGB up to 1366x768p60 or 1280x800p60.
LVDS	≤1	Single channel (4-lane), supporting 720p60, up to 1366x768p60 1280x800p60.	**1**	Single channel (4-lane), supporting 720p60, up to 1366x768p60 1280x800p60.
MIPI DSI	≤1	•Supports 1 x 4-channel MIPI DSI display with pixels from LCDIF;	**1**	•Supports 1 x 4-channel MIPI DSI display with pixels from LCDIF;
		• Compatible with MIPI DSI Specification v1.2 and MIPI D-PHY Specification v1.2;;		• Compatible with MIPI DSI Specification v1.2 and MIPI D-PHY Specification v1.2;;
		•Supports resolutions such as 1080p 60 or 1920x1200p60;		•Supports resolutions such as 1080p 60 or 1920x1200p60;
		•The maximum data rate per lane is 1.5 Gbps.		•The maximum data rate per lane is 1.5 Gbps.

SAI	≤3	• The SAI module provides a Synchronous Audio Interface (SAI); • The SAI1 supports 2 channels, SAI2 supports 4 channels, and SAI3 supports 1 channel; • Supports full - duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.	**1**	The sampling rate supports 8kHz to 384kHz.
JTAG	≤1	The JTAG interface is led out through 2 x 4 2.54mm spacing pin from the development board.	**1**	The JTAG interface is led out through 2 x 4 2.54mm spacing pin from the development board.
SD/SDIO	≤2	uSDHC1 is used internally on the SoM; uSDHC2 is a 4 - bit SD card 3.0, compatible with 200MHz SDR signaling and supporting speeds up to 100MB/s; uSDHC3 is a 4 - bit SDIO3.0	**2**	The uSDHC2 is 4-bit SD card 3.0 compatible with 200 MHz SDR signaling and supports up to 100MB/sec; the uSDHC3 is 4-bit SDIO 3.0.
USB	≤2	There are 2 x USB 2.0 controllers with integrated PHYs that support master-slave switching.	**2**	There are 2 x USB 2.0 controllers with integrated PHYs that support master-slave switching.
I3C	≤2	Two modified integrated circuit (I3C) modules. The I3C is a serial interface for connecting peripheral devices and application processors. Supports 400Kbit/s Fast Mode and 1000Kbit/s Fast Mode Plus. Backward compatible with I2C.	/	
SPI	≤8	Supports master-slave mode configuration.	/	
I2C	≤8	The maximum supported data rate is 100 Kbit/s in the standard mode;	**3**	The maximum supported data rate is 100 Kbit/s in the standard mode;
		The maximum speed supported in fast mode is 400Kbit/s;		The maximum speed supported in fast mode is 400Kbit/s;
		The maximum supported data rate is 1000 Kbit/s in the enhanced fast mode;		The maximum supported data rate is 1000 Kbit/s in the enhanced fast mode;
		The maximum supported data rate is 3400 Kbit/s in the high - speed		The maximum supported data rate is 3400 Kbit/s in the high - speed

		mode; The maximum supported data rate is 5000 Kbit/s in the enhanced fast mode; Supports high-speed mode and ultra-fast mode in slave mode;		mode; The maximum supported data rate is 5000 Kbit/s in the enhanced fast mode; Supports high-speed mode and ultra-fast mode in slave mode;
UART	≤8	Baud rate up to 5Mbps.	/	
CAN-FD	≤2	The CAN-FD module is a CAN protocol controller compliant with ISO11898-1 and CAN 2.0B.	**1**	The CAN-FD module is a CAN protocol controller compliant with ISO11898-1 and CAN 2.0B.
MQS	≤2	MQS (Medium Quality Sound) is used to generate mediate-quality audio via GPIO. It allows users to connect stereo speakers or headphones to a power amplifier without an additional audio chip.	/	
ADC	≤4	The ADC is a 12-bit, 4-channel, 1MS/s ADC.	**4**	The ADC is a 12-bit, 4-channel, 1MS/s ADC.
PDM	≤3	It is a 24-bit PDM module with linear phase response that supports high AOP microphones for audio quality applications.	/	
TPM	≤6	Timer/PWM Module 16-bit counter supporting free-running or modulo count modes, with up or down counting capability. Configurable for multiple functions: Input Capture, Output Compare, Edge-Aligned PWM, or Center-Aligned PWM.	**3**	Timer/PWM Module 16-bit counter supporting free-running or modulo count modes, with up or down counting capability. Configurable for multiple functions: Input Capture, Output Compare, Edge-Aligned PWM, or Center-Aligned PWM.

Note: The maximum number of parameters in the table is the theoretical value of hardware design or CPU; The number of interface resources defined by UP4 in the table is the maximum number supported by the UP4 universal package.

SoM Appearance & Parameters:



* Note: The dimensional tolerance is ±0.2mm.

Software Support:

OS	Linux 6.1+Qt 6.5.0
Flashing method	• TF Card Flashing •USB OTG Flashing

Product Materials:

Linux6.1 Materials List:	User manual, compilation guide manual, Linux kernel source code, file system, factory image, VM Ubuntu image for the development environment, programming tool, source code of QT test routines*, application notes*
Hardware Documentation List:	Hardware manual, source file of the baseboard schematic diagram (AD format), source file of the baseboard PCB (AD format), PDF of the baseboard schematic diagram, data sheet, 2D CAD drawing of the core board, 2D CAD drawing of the baseboard, pin function multiplexing table, design guidance*

Note: The documentation will be gradually provided and enriched after the product is released.

Ordering Model List:

Specification Model	Core	CPU Clock	RAM	ROM	Operating Temperature	Supply
FET-MX9352-UP4+171GSE8GIxx:xx	2×A55	A55@1.7GHz	1GB	8GB	-40℃~+85℃	Mass Production

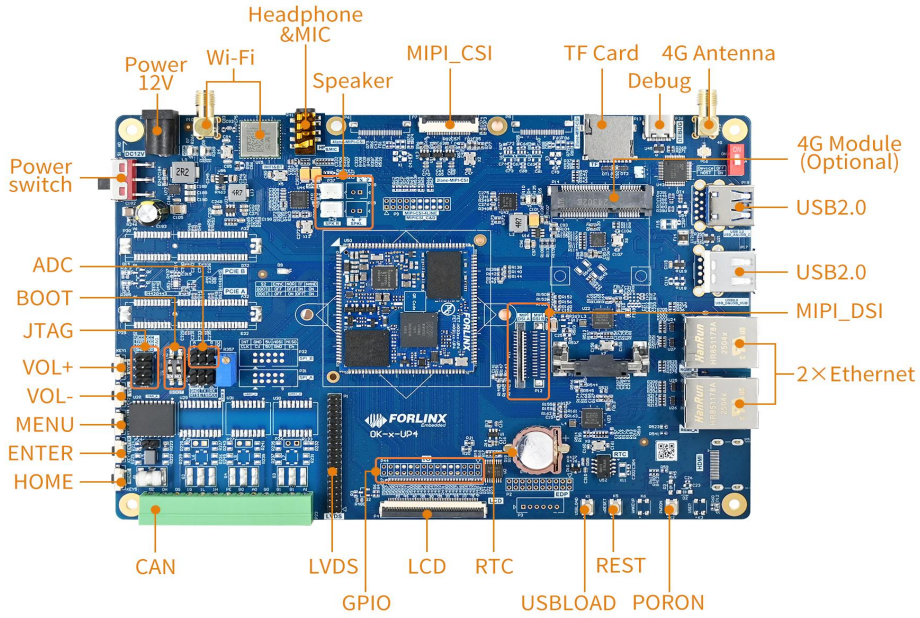
SoM Naming Rules:

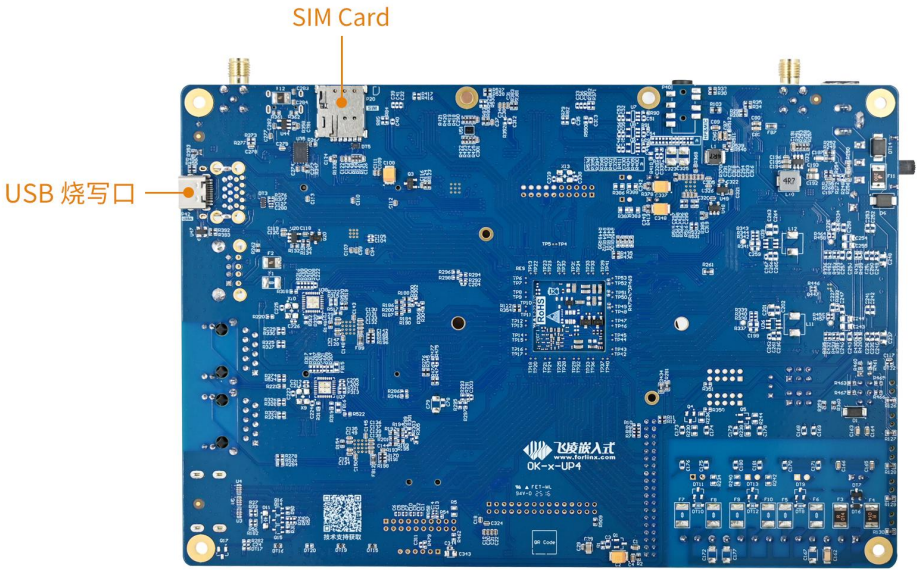
A	B	C	-	D	+	E	F	G	H	I	J	K	:	L	M

This table describes SoM number terms to define its characteristics (e.g., CPU, frequency, temperature grade, version).

Field	Field Description	Value	Description
A	Grade	PC	Prototype Sample
		Blank	Mass Production
B	Product Line Identification	FET	Forlinx Embedded SoM
-	Segment Identification	-	
C	CPU Name	MX9352	i.MX9352
-	Segment Identification	-	
D	Connection	UP4	LCC+LGA general package dimension 40mm×40mm
+	Segment Identification	+	The configuration parameter section follows this identifier.
E	CPU Clock	17	1.7 GHz
F	RAM Capacity (Unit: Byte)	1G	1GB
		512	512MB
G	Single ROM Type	SN	Nand Flash
		SE	eMMC
H	Single ROM Capacity (Unit: Byte)	256	256MB
		8G	8GB
I	Operating Temperature	C	0 to 70℃ Commercial-grade
		I	-40 to 85℃ Industrial-grade
J	Configuration No.	A~Z	If the E ~ I field values of each product are the same, the field values are the same, in ascending order according to the configuration release time
K	PCB Version	10	V1.0
		xx	Vx.x
:LM	Internal Identification of the Manufacturer	: xx	This content is an internal manufacturer's marking and has no impact on usage.

Development Board:





Development Board Function Parameters:

Function	Quantity	Parameter
WiFi	1	Single antenna 2.4G & 5GHz Wi-Fi Dual-band 1X1 802.11ac+Bluetooth 4.2
Bluetooth	1	
Audio	1	Dual - channel speaker interface, class - D, 1.3W; Stereo headphone output, 32Ohm load; Headphone recording
MIPI-CSI	1	Led out from the FPC socket, 2lane
TF Card	1	Data rate up to SDR104;
4G	1	Supports 4G modules with a miniPCIE interface, integrating USB2.0 communication signals.
UART Debug	1	Integrated into a single Type-C port, enabling connection to a PC for debugging.
USB2.0	2	1 x USB-D native USB2.0 and 1 x USB-HUB are led out
Ethernet	2	2 x Gigabit ports led out via a standard RJ45 socket
MIPI-DSI	1	4-lane MIPI-DSI Screen, support capacitive touch and backlight adjustment Single lane maximum resolution 1920 × 1080 @ 60Hz
RTC	1	On-board CR1220 battery, keep going when power is off
		RGB888 interface, supporting capacitive touch and resistive touch, and allowing backlight brightness adjustment. The maximum resolution is 1280×800.
LVDS	1	4-lane LVDS, supporting capacitive touch screen and backlight brightness adjustment, up to 1280×800@60Hz
CAN	1	Supports CAN2.0, electrical quarantine
ADC	3	Led out from the pin header and can be connected to the on-board sliding rheostat
UART	1	5 x UART, led out through pin headers.
BOOT	1	BOOT mode selection configuration
JTAG	1	JTAG, led out through pin
KEY ADC	5	5 keys are led out via 1 x LRADC

Note: The parameters in the table are the theoretical values of hardware design or CPU.

Power Consumption:

No.	Test Item	SoM Power (W)	Development Board Power (including SoM)
1	No-load starting peak power consumption	1.6 W	2.54W
2	Sleep power consumption	0.038 W	1.27W
3	No-load standby power consumption	0.735 W	0.49W
4	USB read and write power	0.87 W	2.03W
5	TF read and write power	1.175 W	1.74W
6	4G module PING network power consumption	0.76 W	2.26W
7	WiFi module PING network power consumption	0.71 W	1.28W
8	7-inch LCD screen power consumption	0.79 W	3.6W
9	10-inch LVDS screen power consumption	0.79 W	5.46W
10	7-inch MIPI screen video playback power	0.77 W	4.42W
11	CPU pressure + memory pressure + eMMC read/write pressure test power	1.47 W	2.08W

