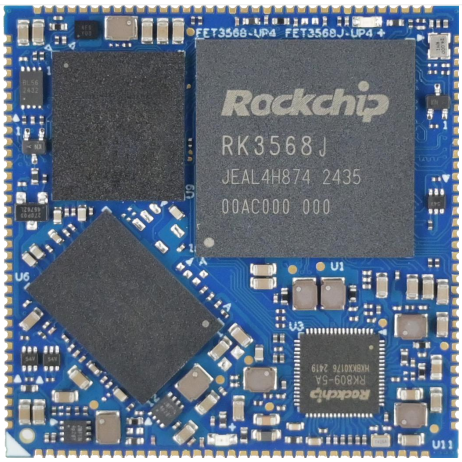
# FET3568-UP4 / FET3568J-UP4 SoM

FET3568-UP4/FET3568J-UP4 SoMs are developed and designed based on Rockchip RK3568B2 and RK3568J processors respectively, which are high-performance, low-power and feature-rich application processors built by Rockchip for AIoT and industrial markets. Features a quad-core 64-bit Cortex-A55 architecture running at up to 2.0 GHz with a built-in NPU. The SoM enhances the exposure of the processor's functional pins, allowing for evaluation and secondary development. It has undergone thorough environmental, stability, and aging tests to guarantee reliable and stable operation.



FET3568J-UP4 SoM

| | | |
|---|---|---|
| 4×Cortex-A55<br>Architecture | 2.0 GHz<br>Clock | UP4 package<br>Compatibility |
| ARM-G52-2EE<br>GPU | 1TOPS<br>NPU | PCIE, USB3.0<br>High-speed Interface |

## Product Features:

- Supports 38.4 GFLOPs 800MHz GPU Mali-G52;
- Built-in 1TOPS NPU, suitable for AI edge computing applications;
- Integrated Image Signal Processor (ISP), supporting 2 x MIPI-CSI camera interfaces;
- Rich high-speed interfaces supported, including 2×USB 3.0, 2×PCIe 3.0, and 3×SATA 3.0;
- Multiple display interfaces supported: HDMI (up to 4K output), LVDS, MIPI-DSI, RGB, and eDP, with triple-screen same-display or independent-display capabilities;
- Supports dual gigabit Ethernet;
- LCC+LGA package (compact size);
- Universal package and is compatible with the UP4 series of SoMs.

## SoM Parameter:

| | |
|---|---|
| **Processor** | **Rockchip RK3568B2 / RK3568J**<br>CPU: Quad-coreCortex-A55@2.0GHz / 1.8GHz<br>NPU: 1TOPS, supporting INT8/INT16/FP16/BFP16 mixing operation<br>GPU: Mali-G52-2EE; OpenGL ES 1.1, 2.0, 3.2, Vulkan 1.0,1.1, OpenCL 2.0<br>VPU:<br>Hardware Decoding:<br>• H.264, H.265, VP9: up to 4096x2304@60fps<br>• VP8: up to 1920x1088@60fps<br>• VC1, MPEG-4, MPEG-2, MPEG-1: up to 1920x1088@60fps<br>• H.263: up to 720x576@60fps<br>Hardware Encoding:<br>• H.264/AVC, H.265/HEVC: up to 1920×1080@60fps |
| **RAM** | 1GB/2GB/4GB/8GB LPDDR4X |
| **ROM** | 8GB/16GB/32GB/64GB eMMC |
| **Operating Temperature** | DC 5V |
| **Working Voltage** | -40℃ ~ +85℃/0℃ ~ +80℃ |
| **Connection** | LCC + LGA (487 pins, pin center pitch of stamp hole is 1mm, single pin size: 0.7 * 0.6mm, ball pitch of LGA is 1.27 mm, single ball diameter is 0.8mm) |

## SoM Function Parameters:

| Function | Maximum Number | Parameter | UP4 defines the number of interface resources | Parameter |
|---|---|---|---|---|
| **MIPI-DSI** | 2 | 2 x 4 - lane MIPI display serial interfaces, supporting MIPI V1.2 version. The maximum resolution of a single channel is 1920×1080@60Hz, and the maximum resolution of dual channels is 2560×1600@60Hz. | 1 | 1 x 4 - lane MIPI display serial interfaces, supporting MIPI V1.2 version. The maximum resolution of a single channel is 1920×1080@60Hz, and the maximum resolution of dual channels is 2560×1600@60Hz. |
| **HDMI** | 1 | Supports HDMI 2.0 with resolutions up to 1080p @ 120Hz or 4096 × 2304 @ 60Hz | 1 | Supports HDMI 2.0 with resolutions up to 1080p @ 120Hz or 4096 × 2304 @ 60Hz |
| **LVDS** | 1 | Single lane（4 lanes）supports 1280×800@60Hz | 1 | Single lane（4 lanes）supports 1280×800@60Hz |

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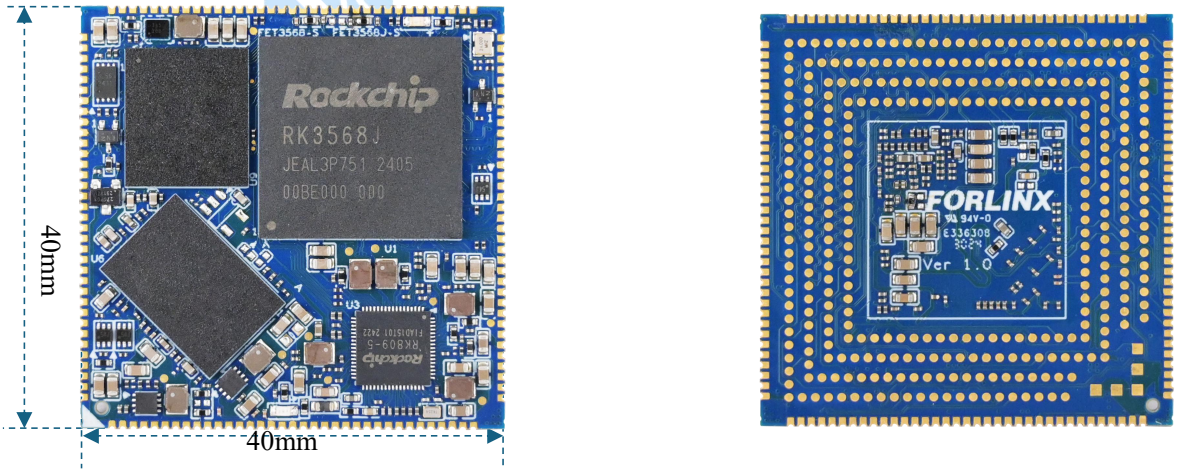
|---|---|---|---|---|
| **eDP** | 1 | 1 x 4-lane eDP display interface, supporting eDP V1.3, and the maximum resolution is 2560×1600@60Hz | 1 | 1 x 4-lane eDP display interface, supports eDP V1.3, and the maximum resolution is 2560×1600@60Hz |
| **RGB** | 1 | Supports RGB 888, maximum resolution 1280 x 800 | 1 | Supports RGB 888, maximum resolution 1280 * 800 |
| **Camera** | 3 | Supports 1 x 4 Lanes MIPI-CSI, 2 x 2Lanes MIPI-CSI | 2 | Supports 2 x 2Lanes MIPI-CSI |
| **IIS** | ≤4 | 1×8ch I2S/TDM, 2×2ch I2S, 1×8ch PDM | / | |
| **Audio** | 1 | Built - in codec, which directly outputs audio analog signals with a sampling rate ranging from 48KHz to 192KHz: Mono speaker, class - D, 1.3W; Stereo headphone output with a 32Ohm load; one differential MIC input. | 1 | Built - in codec, which directly outputs audio analog signals with a sampling rate ranging from 48KHz to 192KHz: Mono speaker, class - D, 1.3W; Stereo headphone output with a 32Ohm load; one differential MIC input. |
| **SDIO** | ≤2 | SDIO 3.0 with up to 104MB/S data throughput | 2 | SDIO 3.0 with up to 104MB/S data throughput |
| **Ethernet** | ≤2 | 2 x GMAC, RGMII/RMII interface are routed out | 2 | 2 x GMAC, RGMII/RMII interface are routed out |
| **USB 2.0** | 2 | USB 2.0 Host, independent port, not multiplexed with USB 3.0 | 2 | USB 2.0 Host, independent port, not multiplexed with USB 3.0 |
| **USB 3.0** | 2 | 1 x USB 3.0 Host port, which can be used independently as a USB 2.0 Host; 1 x USB 3.0 OTG port, which can be used independently as a USB 2.0 OTG. | 2 | 1 x USB 3.0 Host port, which can be used independently as a USB 2.0 Host; 1 x USB 3.0 OTG port, which can be used independently as a USB 2.0 OTG. ; |
| **SATA** | ≤3 | SATA 3.0 up to 6.0 Gb/s with eSATA support | / | |
| **PCIe2.1** | ≤1 | PCIe 2.1×1, up to | 1 | PCIe 2.1×1, up to 5.0Gbps, RC mode |

| | | | | |
|---|---|---|---|---|
| | | 5.0Gbps，RC mode | | |
| **PCIe3.0** | ≤2 | PCIe 3.0，1×2Lanes or 2×1Lane, up to 8.0 Gbps per Lane; 1Lane supports Root Complex (RC) mode only; 2 Lanes supports Root Complex (RC) and End Point (EP) model. | 1 | PCIe 3.0, 1x2Lanes, up to 8.0 Gbps per Lane; 1Lane supports Root Complex (RC) mode only; 2Lanes supports Root Complex (RC) and End Point (EP) model. |
| **UART** | ≤10 | Up to 4Mbps | 3 | Up to 4Mbps |
| **CAN** | ≤3 | Supports CAN2.0 B up to 1Mbps | 2 | Supports CAN2.0 B up to 1Mbps |
| **SPI** | ≤4 | Support master & slave mode, with configurable software | / | |
| **I2C** | ≤5 | Supports 7bits and 10bits address modes up to 1 Mbit/s | 3 | Supports 7bits and 10bits address modes up to 1 Mbit/s |
| **PWM** | ≤16 | 32bits timer/counter | 4 | 32bits timer/counter |
| **FSPI** | ≤1 | Supports serial NOR Flash/NAND Flash and Boot | / | |

**Note: The maximum number of parameters in the table is the theoretical value of hardware design or CPU; The number of interface resources defined by UP4 in the table is the maximum number supported by the UP4 universal package.**

## Appearance & Dimension:




**Note: PCB thickness is 1.2mm; total height of PCBA is 3.2mm; dimensional tolerance is ± 0.2mm.**

## Software Support:

| | |
|---|---|
| **OS** | Linux5.10+Qt5.15.8 |
| **System flashing Method** | • SD card<br>• USB OTG |

## Peripheral Support List:

| | **Interface** | **Function** | **Solution** |
|---|---|---|---|
| **Linux5.10 Drive Support List** | IIC | Capacitive touch | FT5x06 |
| | IIC | Capacitive touch | GT928 |
| | IIC | RTC | PCF8563T |
| | SDIO | Wi-Fi | AW-CM358SM |
| | UART | BT | |
| | USB | UVC camera | Logitech C270 |
| | USB | 4G | Quectel EM05-CE R2.0 (driver compatible with EC20-[illegible]) |
| | USB | 5G | Quectel RM500U |
| | USB | USB to 4-port serial port | XR21V1414 |
| | MIPI-CSI | Camera | OV13850 |
| | PCIe | Gigabit Ethernet | FIT-RTL8111F_PCIE_V1.0 |
| | MIPI-DSI | 7-inch LCD | FT5x06d capacitive touch, 1024 × 600 resolution |
| | LVDS | 10.1-inch LCD | FIT_LVDS10.1C_V2.0， GT928 capacitive touch， |
| | eDP | 12.5-inch LCD | BOE NV125FHM-N82， 1920×1080 resolution |
| | RGMII | Gigabit Ethernet | RTL8211FSI-CG |
| | PWM | LCD Backlight | General |
| | UART | General | General |
| | SPI | General | General |
| | GPIO | General | General |

## Product Documentations List:

| | |
|---|---|
| **Linux5.10 Documentation List:** | User Manual, Compilation Guide, Linux Kernel Source Code, File System, Factory Image, Development Environment VM Ubuntu Image, FTP Tool, YUV Video Playback Tool, Camera Test Tool, SD Flash Card Creation Tool, USB OTG Flash Tool, Mass Production Programming Tool, Driver Installation Tool, Firmware Flash Tool, Serial Port Driver Installation Tool, QT Test Routine Source Code, Application Notes. |
| **Hardware Documentation List:** | Hardware Manual, Hardware Design Guide, Pin Function Multiplexing Table, SoM 3D Diagram (STEP), Data Sheet, Carrier Board Schematic Source File (AD Format), Carrier Board PCB Source File (AD Format), Carrier Board Schematic PDF, SoM 2D CAD Diagram, Carrier Board 2D CAD Diagram. |

**Note: The documentation will be gradually provided and enriched after the product is released.**

## Order Model List:

| Specification Model | Core | CPU Clock | RAM | ROM | Operating Temperature | Supply |
|---|---|---|---|---|---|---|
| FET3568J-UP4+182GSE16GIxx: xx | 4×A55 | 1.8 GHz | 2GB | 16GB | -40~+85℃ | Mass Production |
| FET3568J-UP4+184GSE32GIxx: xx | 4×A55 | 1.8 GHz | 4GB | 32GB | -40~+85℃ | Mass Production |
| FET3568-UP4+202GSE32GCxx: xx | 4×A55 | 2.0 GHz | 2GB | 32GB | 0~+80℃ | Mass Production |
| FET3568-UP4+201GSE32GCxx: xx | 4×A55 | 2.0 GHz | 1GB | 32GB | 0~+80℃ | Mass Production |

## SoM Naming Rules:

| A | - | B | - | C | + | D | E | F | G | H | I | J | : | K | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

This table describes SoM number terms to define its characteristics (e.g., CPU, frequency, temperature grade, version).

| Field | Field Description | Value | Description |
|---|---|---|---|
| A | Product Line Identification | FET | Forlinx Embedded SoM |
| | | FL | Forlinx Embedded All in One Panel |
| B | CPU Name | 3568 | RK3568B2 |
| | | 3568J | RK3568J |
| - | Segment Identification | - | |
| C | Connection | UP4 | LCC+LGA general package dimension 40mm×40mm |
| + | Segment Identification | + | The configuration parameter section follows this identifier. |
| D | CPU Clock | 18 | 1.8 GHz |
| | | 20 | 2.0 GHz |
| E | RAM Capacity (Unite：Byte) | 1G | 1GB |
| | | 2G | 2GB |
| | | 4G | 4GB |
| | | 8G | 8GB |
| F | Single ROM Type | SE | eMMC |
| G | Single ROM Capacity (Unite：Byte) | 8G | 8GB |
| | | 16G | 16GB |
| | | 32G | 32GB |
| | | 64G | 64GB |
| H | Running temperature | C | 0 to 80℃ Commercial-grade |
| | | I | -40 to 85℃ Industrial-grade |
| I | Configuration No. | A~Z | If the D ~ H field values of each product are the same, the field values are the same, in ascending order according to the configuration release time |
| J | PCB Version | 10 | V1.0 |
| | | 11 | V1.1 |
| | | xx | Vx.x |

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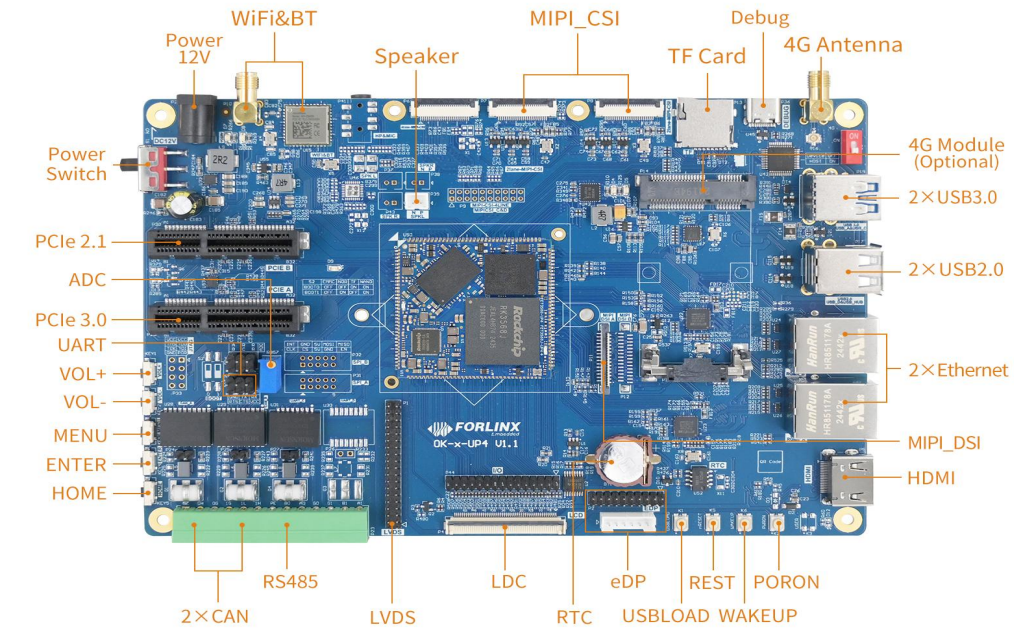
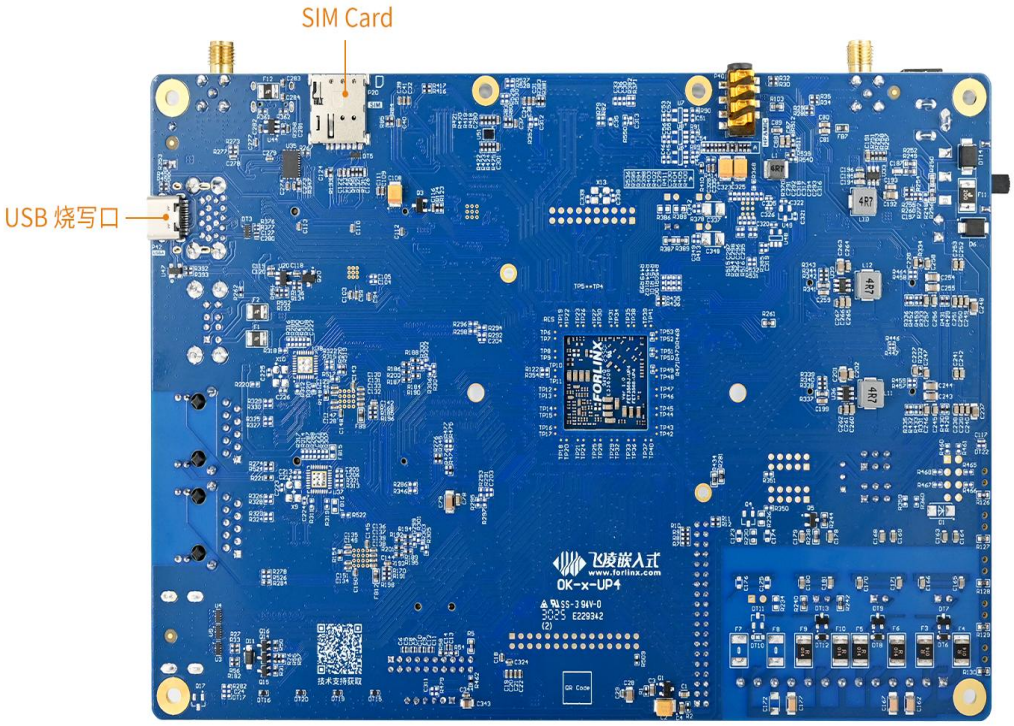
|---|---|---|---|
| : KL | Internal Identification of the Manufacturer | : xx | It is manufacturer's internal logo without influence on use. |

## Development Board:



## Development Board Function Parameters:

| Function | Quantity | Parameter |
|---|---|---|
| **WiFi** | 1 | Single antenna 2.4G & 5GHz Wi-Fi Dual-band 1X1 802.11ac +Bluetooth 4.2 |
| **Bluetooth** | 1 | |
| **Audio** | | Mono speaker connector, class-D, 1.3 W; Stereo headphone output, 32 Ohm load; Headphone recording + on-board MIC recording |
| **MIPI-CSI** | 3 | Led out from the FPC socket, 4lane+ 2lane+ 2lane |
| **TF Card** | 1 | Data rate up to SDR104; |
| **4G** | 1 | Supports 4G modules with a miniPCIE interface, integrating USB2.0 communication signals. |
| **UART Debug** | 2 | Integrated into a single Type-C port, enabling connection to a PC for debugging. |
| **USB3.0** | 2 | USB _ A can switch the master-slave mode and perform USB programming, while USB _ C only supports the master mode. |
| **USB2.0** | 2 | 1 x USB-D native USB2.0 and 1 x USB-HUB are led out |
| **Ethernet** | 2 | 2 x Gigabit ports led out via a standard RJ45 socket |
| **HDMI** | 1 | Supports HDMI 2.1 resolution up to 4096× 2304 @ 60Hz |
| **EDP** | 1 | Supports eDP 1.3 resolution up to 2560× 1600 @ 60Hz |
| **MIPI-DSI** | 1 | 4-lane MIPI-DSI, supporting capacitive touch screen and backlight brightness adjustment. The maximum resolution of a single channel is 1920 × 1080@60Hz, and the maximum resolution of dual channels is 2560×1600@60Hz. |
| **RTC** | 1 | On-board CR1220 battery, keep going when power is off |
| **LCD** | 1 | RGB888 interface, supporting capacitive touch and resistive touch, and allowing backlight brightness adjustment. The maximum resolution is 1280×800. |
| **LVDS** | 1 | 4-lane LVDS, supporting capacitive touch screen and backlight brightness adjustment, up to 1280×800@60Hz |
| **RS485** | 1 | Electrical quarantine |
| **CAN** | 2 | Supports CAN2.0B, electrical quarantine |
| **ADC** | 3 | Led out from the pin header and can be connected to the on-board sliding rheostat |
| **UART** | 1 | 5 x UART, led out through pin headers. |
| **KEY ADC** | 5 | 5 keys are led out via 1 x LRADC |
| **PCIe** | 2 | PCIe _ B 2.1, can only do RC mode, PCIe _ A 3.0, can do EP and RC mode |

**Note: The parameters in the table are the theoretical values of hardware design or CPU.**

## Power Consumption:

| No. | Test Item | SoM Power (W) | Development Board Power (including SoM) |
|---|---|---|---|
| 1 | No-load starting peak power consumption | 3.45 W | 5.304W |
| 2 | Sleep power consumption | 1.295 W | 0.636W |
| 3 | No-load standby power consumption | 1.295 W | 2.7W |
| 4 | USB read and write power | 1.47 W | 3.312W |
| 5 | TF read and write power | 1.845 W | 3.36W |
| 6 | 4G module PING network power | 1.44 W | 3.504W |
| 7 | WiFi module PING network power | 1.31 W | 2.688W |
| 8 | 7-inch LCD screen video playback power | 1.55 W | 5.244W |
| 9 | 10-inch LVDS screen video playback | 1.65 W | 6.648W |
| 10 | 7-inch MIPI screen video playback power | 1.94 W | 5.568W |